Eric Rotenberg

E-mail & Home Page	Phone	Dept. Address	Home Address
ericro@cs.wisc.edu	office: (608)265-3826	1210 W. Dayton St.	618 1/2 S. Mills St.
www.cs.wisc.edu/~ericro/ericro.html	home: (608)259-9197	Madison, WI 53706	Madison, WI 53715

OBJECTIVE

My objective is to perform research in the area of *high-performance computer architecture* and teach in the broader areas of computer science and electrical and computer engineering. High-performance computer architecture specifically deals with building fast general-purpose and special-purpose computer systems, including hardware -- processors, memory, and input/output -- and advanced compilers.

EDUCATION

University of Wisconsin - Madison

8/99 (expected) PhD - Computer Sciences (computer architecture)

5/96 MS - Computer Sciences (GPA: 4.0)

12/91 BS - Electrical Engineering (GPA: 3.7)

EXPERIENCE

University of Wisconsin - Madison

1/95 - present **Research Assistant.**
Advisor: Professor James E. Smith
Thesis: "Trace Processors"

In my thesis, I explore the trace processor microarchitecture, a processor organized entirely around *traces* -- dynamic instruction sequences, 16 to 32 instructions in length, which embed any number of taken or not-taken branch instructions. The trace processor looks far ahead into the program to search for instructions that may execute in parallel, thus exposing parallelism in apparently-serial programs. Constructing the large "instruction window" for exposing parallelism is normally complex, but trace processors use hierarchy to manage this complexity. Traces provide the hierarchy -- rather than work at the granularity of individual instructions, the processor efficiently sequences through the program at the higher level of traces and allocates trace-sized units of work to distributed resources.

9/95 - 9/98 **Microarchitect and designer.** Kestrel Multiscalar Project
Microarchitecture definition, design, and timing of a prototype Multiscalar processor.

9/94 - 12/94 **Teaching Assistant.** Computer lab course

2/92 - 8/94 IBM - Rochester, MN
AS/400 Processor Development Lab
Starting Title: Engineer / Ending Title: Associate Engineer

Logic Designer. Worked on the design of three different chips comprising the AS/400 processor. (The AS/400 is a mid-range computer for enterprise solutions.) Worked through all phases of the chip design process, from high-level definition through logic design, synthesis, simulation, and timing. Owned the timing process for one of the chip design teams.

HONORS

- Best Paper Award, MICRO-30: "Trace Processors" (1997)
- IBM Graduate Fellowships (1995-98)
- Intel/UW-Madison VLSI Design Contest Winner (1995)
- UW-Madison Computer Sciences Dept.: Summer Research Assistantship Award (1995)
- IBM Peer Recognition Award: Outstanding Ownership of PIU Timing Verification (1994)
- UW-Madison Deans Honor List (1987-1991)
- Byrd Scholarship (1987-88)
- Knapp Scholarship (1987-88)
- Participated in the Department of Energy Fermilab Program (1987)

Eric Rotenberg

PUBLICATIONS

- "AR-SMT: A Microarchitectural Approach to Fault Tolerance in Microprocessors," Eric Rotenberg, To appear in *29th Fault-Tolerant Computing Symposium*, June 1999.
- "A Trace Cache Microarchitecture and Evaluation," Eric Rotenberg, Steve Bennett, and J. E. Smith, *IEEE Transactions on Computers*, Special Issue on Cache Memory, Feb. 1999.
- "A Study of Control Independence in Superscalar Processors," Eric Rotenberg, Quinn Jacobson, and James E. Smith
  - *5th Annual Int'l Symposium on High Performance Computer Architecture*, Jan. 1999
  - University of Wisconsin-Madison Technical Report #1389, Dec. 1998
- "Trace Processors," Eric Rotenberg, Quinn Jacobson, Yiannakis Sazeides, and James E. Smith, *30th Annual International Symposium on Microarchitecture*, Dec. 1997.
- "Path-Based Next Trace Prediction," Quinn Jacobson, Eric Rotenberg, and James E. Smith, *30th Annual International Symposium on Microarchitecture*, Dec. 1997.
- "Assigning Confidence to Conditional Branch Predictions," Erik Jacobsen, Eric Rotenberg, and James E. Smith, *29th Annual International Symposium on Microarchitecture*, Dec. 1996.
- "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching," Eric Rotenberg, Steve Bennett, and James E. Smith
  - *29th Annual International Symposium on Microarchitecture,* Dec. 1996
  - University of Wisconsin-Madison Technical Report #1310, April 1996

TALKS

- Wisconsin Computer Architecture Industry Affiliates Program
  Audience: Chief technical representatives from Intel, IBM, HP, Compaq/DEC, Sun, SGI/Cray, Ross Technology, National Semiconductor, TI, and AMD
  1996 - The Trace Cache
  1997 - Trace Processors
  1998 - Control Independence
- IBM in Rochester, MN with audio link to IBM in Endicott, NY
  Audience: site-wide, diverse technical audience
  1996 - The Trace Cache
  1997 - Trace Processors
- Computer Architecture Conferences
  1996 - MICRO-29: (1) The Trace Cache (2) Branch Confidence Mechanisms
  1997 - MICRO-30: Trace Processors
  1999 - HPCA-5: Control Independence
- 5 seminars given in the UW Computer Sciences Dept. and Dept. of Elec. and Comp. Engr.

REFERENCES

Professor James E. Smith
Dept. of Electrical and Computer Engr.
University of Wisconsin-Madison
1415 Engineering Drive
Madison, WI 53706-1691
jes@ece.wisc.edu
(608)265-5737

Professor Gurindar S. Sohi
Computer Sciences Department
University of Wisconsin-Madison
1210 West Dayton Street
Madison, WI 53706-1691
sohi@cs.wisc.edu
(608)262-7985

Professor Kewal K. Saluja
Dept. of Electrical and Computer Engr.
University of Wisconsin-Madison
1415 Engineering Drive
Madison, WI 53706-1691
saluja@engr.wisc.edu
(608)262-6490

John Borkenhagen
International Business Machines
Department 49GA
3605 Highway 52 North
Rochester, MN 55901
bork@us.ibm.com
(507)253-0755