Reading Assignment

- Read Assignment #2.
- Read George and Appel's paper, "Iterated Register Coalescing." (Linked from Class Web page)
- Read Larus and Hilfinger's paper, "Register Allocation in the SPUR Lisp Compiler."

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LiveIn and LiveOut are computed, using the following rules:

- 1. If Basic Block b has no successors then LiveOut(b) = false
- 2. For all Other Basic Blocks

 $LiveOut(b) = \bigvee_{s \in Succ(b)} LiveIn(s)$

3. LiveIn(b) =

If V is used before it is defined in Basic Block b Then true Elsif V is defined before it is used in Basic Block b Then false Else LiveOut(b)

Liveness Analysis

Just because a definition reaches a Basic Block, b, *does not* mean it must be allocated to a register at b.

We also require that the definition be *Live* at b. If the definition is dead, then it will no longer be used, and register allocation is unnecessary.

For a Basic Block b and Variable V: Liveln(b) = true if V is Live (will be used before it is redefined) at the beginning of b.

LiveOut(b) = true if V is Live (will be used before it is redefined) at the end of b.

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Merging Live Ranges

It is possible that each Basic Block that contains a definition of v creates a *distinct* Live Range of V.

∀ Basic Blocks, b, that contain a definition of V:

 $\begin{array}{l} Range(b) = \\ \{b\} \cup \{k \mid b \in DefsIn(k) \ \& \ LiveIn(k)\} \end{array}$

This rule states that the Live Range of a definition to V in Basic Block b is b plus all other Basic Blocks that the definition of V reaches and in which V is live. 98





Li=F **Di={}** 1 x← Do={1} Lo=T ={1} Di={1} Li=F 2 Li=T 3 x← Lo=T Do={2} Do={1} Lo=T Di={1,2} Li=T $\mathbf{x} \rightarrow$ Lo=F **Do={1,2}** Di={1,2,5,6} Li=F x↔ Lo=T Do={5} Li=F 6 Di={5} x← Do={6} Di={5,6} Li=T $\mathbf{x} \rightarrow$ Lo=F Do={5,6} Di={5,6} Li=F Lo=F Do={5,6}

The Live Ranges we Compute are Range(1) = $\{1\} \cup \{3,4\} = \{1,3,4\}$ Range(2) = $\{2\} \cup \{4\} = \{2,4\}$ Range(5) = $\{5\} \cup \{7\} = \{5,7\}$ Range(6) = $\{6\} \cup \{7\} = \{6,7\}$ Ranges 1 and 2 overlap, so Range(1) = Range(2) = $\{1,2,3,4\}$ Ranges 5 and 6 overlap, so Range(5) = Range(6) = $\{5,6,7\}$

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Interference Graph Example An Interference Graph represents int p(int lim1, int lim2) { for (i=0; i<lim1 && A[i]>0;i++){} interferences between Live Ranges. for (j=0; j<lim2 && B[j]>0;j++){} return i+j; } Two Live Ranges *interfere* if they share one or more Basic Blocks in We optimize array accesses by placing common. **εA**[0] and **εB**[0] in temporaries: int p(int lim1, int lim2) { Live Ranges that interfere *must* be int *T1 = &A[0]; allocated different registers. for (i=0; i<lim1 && *(T1+i)>0;i++){} int *T2 = &B[0]; for (j=0; j<lim2 && *(T2+j)>0;j++){} return i+j; In an Interference Graph: } Nodes are Live Ranges • lim1 lim2 An undirected arc connects two Live Ranges if and only if they interfere т1 т2 i j

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Register Allocation via Graph Coloring

We model global register allocation as a Coloring Problem on the Interference Graph

We wish to use the fewest possible colors (registers) subject to the rule that two connected nodes can't share the same color.

Optimal Graph Coloring is NP-Complete

Reference:

"Computers and Intractability," M. Garey and D. Johnson, W.H. Freeman, 1979.

We'll use a Heuristic Algorithm originally suggested by Chaitin et. al. and improved by Briggs et. al.

References:

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"Register Allocation Via Coloring," G. Chaitin et. al., Computer Languages, 1981.

"Improvement to Graph Coloring Register Allocation," P. Briggs et. al., PLDI, 1989.

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Since no node has fewer than 3 neighbors, we remove a node based on the minimum Cost/Neighbors value.

lim2 is chosen. We now have:



Remove (say) lim1, then T1, T2, j and i (order is arbitrary).

