Worksheet 7 - Cache Memories

Due: April 1st 2016 (Friday) in class

1. Gerald's computer (francisco.cs.wisc.edu) has the following cache parameters for its CPU caches. Fill in the missing parameters in the table below. Recall that C is the cache size (number of data bytes), B is the block size in bytes, E is the number of cache lines per set, and S is the number of cache sets.

   NOTE: 1 KB = 1024 bytes and 1 MB = 1024 KB

   Cache size (C) = S x E x B

Cache Type	C	S	E	B
L1 cache (data)	32 KB	64	8	
L1 cache (instruction)		128	4	64
L2 cache	256 KB		8	64
L3 cache	8 MB	8192		64

2. The following table gives the parameters for a number of different caches. For each cache, fill in the missing fields in the table. Recall that m is the number of physical address bits, C is the cache size (number of data bytes), B is the block size in bytes, E is the associativity (i.e. number of cache lines), S is the number of cache sets, t is the number of tag bits, s is the number of set index bits, and b is the number of block offset bits.

Cache	m	C	B	E	S	t	s	b
1.	32	1024	4	4				
2.	32	1024	4	256				
3.	32	1024	8	1				
4.	32	1024	8	128				

5.	32	1024	32	1				
6.	32	1024	32	4				

3. Assume the following:
   a. The memory is byte addressable.
   b. Memory accesses are to **1-byte words** (not to 4-byte words).
   c. Addresses are 13 bits wide.
   d. The cache is a **direct-mapped cache** (E = 1), with a 4-byte block size (B = 4) and eight sets (S = 8).

The contents of the cache are as follows, with all numbers given in hexadecimal notation.

Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	09	1	86	30	3F	10
1	45	1	60	4F	E0	23
2	EB	0	-	-	-	-
3	06	0	-	-	-	-
4	C7	1	06	78	07	C5
5	71	1	0B	DE	18	4B
6	91	1	A0	B7	26	2D
7	46	0	-	-	-	-

A. The following figure shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

CO - The cache block offset
CI - The cache set index
CT - The cache tag

12	11	10	9	8	7	6	5	4	3	2	1	0

Suppose a program running on the machine references the 1-byte word at address **0x0E34**. Indicate the cache entry accessed and the cache byte value returned in hex. Indicate whether a cache miss occurs. If there is a cache miss, enter "–" for "Cache byte returned."

B. Address Format

12	11	10	9	8	7	6	5	4	3	2	1	0

C. Memory Reference

Parameter	Value
Cache block offset (CO)	0x_____
Cache set index (CI)	0x_____
Cache tag (CT)	0x_____
Cache hit? (Y / N)	
Cache byte returned	0x_____