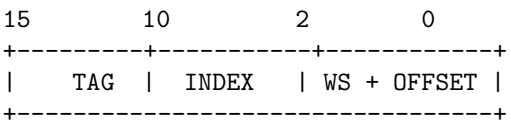
Homework 5 Solutions

CS/ECE 552 Spring 2008

May 12, 2008

Problem 1 and 2 - Direct Mapped Caches and Set associate caches

Cache Layout



Solution to include schematics, state diagram and annotated waveforms. Timing/# of cycles for representative cases should be shown in waveforms. For e.g. cache hit takes 1 cycle, cache miss is 10 cycles etc.

Memory address traces

Simple cases that are to be shown are enlisted below:

1. Simple Cache Hit

W	R	Address	Value	Expected Behaviour
0	1	0x285a	0	Compulsory Miss
0	1	0x286a	0	Compulsory Miss
1	0	0x285e	16	Hit
1	0	0x385c	14	Miss for direct mapped.
1	0	0x285a	10	Hit for 2-way set associative.

2. Simple Cache Miss

W	R	Address	Value	Expected Behaviour
0	1	0xfffc	0	Compulsory Miss
0	1	0x785a	0	Compulsory Miss
0	1	0x4746	0	Compulsory Miss
0	1	0x535e	0	Compulsory Miss

3. Miss on the same index

W	R	Address	Value	Expected Behaviour
1	0	0x385a	0	Compulsory Miss
0	1	0x285a	0	Miss + WB for direct mapped, only miss for 2 way set associative.

4. Miss on same indices

```
W   R   Address  Value Expected Behaviour
1   0   0x385a   20    Compulsory Miss
0   1   0x285a   0     Miss + WB for direct mapped, only miss for 2 way set
associative.
1   0   0x785a   40    Miss + WB for both
```

5. Capacity Miss(Wraps around twice)

```
W   R   Address  Value   Expected Behaviour
0   1   3802     0       Compulsory Miss
0   1   380a     0       Compulsory Miss
0   1   3812     0       Compulsory Miss
0   1   381a     0       Compulsory Miss
0   1   3822     0       .
0   1   382a     0       .
0   1   3832     0       .
0   1   383a     0       .
.
.
.
.
.
.
.
.
0   1   47ea   0         Capacity Miss
0   1   47f2   0         Capacity Miss
0   1   4802   0         Capacity Miss
```

6. Fill the entire cache(All 256 addresses for four banks)

```
W   R   Address  Value   Expected Behaviour
0   1   0        0       Compulsory Miss
0   1   2        0       Conflict Miss
0   1   4        0       Conflict Miss
0   1   6        0       Conflict Miss
0   1   8        0       Compulsory Miss
0   1   a        0       Conflict Miss
0   1   c        0       Conflict Miss
.
.
.
.
.
.
.
.
.
0   1  ff8       0      Compulsory Miss
0   1  ffa       0      Conflict Miss
0   1  ffc       0      Conflict Miss
0   1  ffe       0      Conflict Miss
```

7. Read back trace after writing

```
W   R   Address  Value  Expected Behaviour
1   0   0x385a   0      Compulsory Miss
1   0   0x385a   20     Hit
0   1   0x285a   0      Conflict Miss + WB for direct mapped, only miss for 2 way set
associative.
1   0   0x785a   33     Conflict Miss + WB for both
0   1   0x385a   0      Miss  Student to check if the readback generates a
correct value of 20 from the memory.
0   1   0x285a   0      Miss
0   1   0x785a   0      Miss  Student to check if the readback generates a
correct value of 33 from the memory.
```