

**TUTORIAL – II**  
**ECE 555**  
Updated on September 11<sup>th</sup> 2008

## CADENCE LAYOUT AND PARASITIC EXTRACTION

After finishing a schematic of your design (Tutorial-I), the next step is creating masks which are for fabrication using layout editor, Virtuoso. This tutorial will take you through the steps involved in the creation and layout of designs using standard cell components. This tutorial has two parts. In the first we shall create the layout for an inverter. We shall then do the parasitic extraction and simulate the circuit for post layout analysis. The layers in a layout represent the physical characteristics of the devices and have more details than the schematics. So, in the design flow of your circuit, verification with layout is critical. We will use cells developed by NCSU to layout a simple inverter based on TSMC 0.18um CMOS technology.

- To create layout view of our inverter, go to Library Manager and create a new cell view, as shown in Fig. 1.

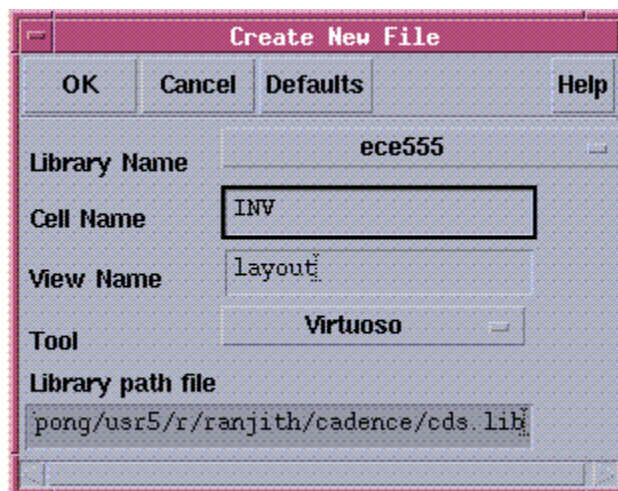


Fig. 1. Creating layout view of inverter

- With click OK, you will see two windows appear, one is *LSW* (Layer Selection Window) and the other is *Virtuoso Layout Editing* window, shown Fig. 2.

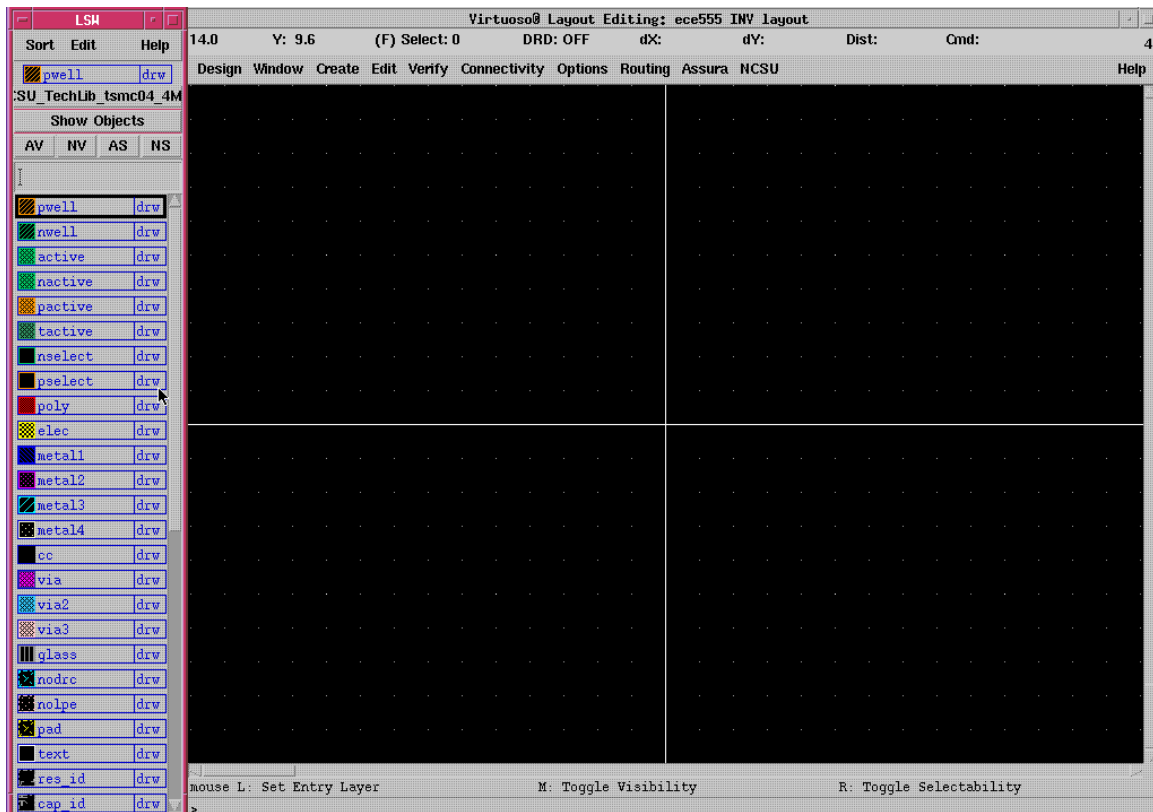


Fig. 2. LSW and Layout Editing window

- To set the display so that all layers will appear, in *Layout Editing* window, select **Options --> Display**. Set the options as Fig. 3 and click OK.

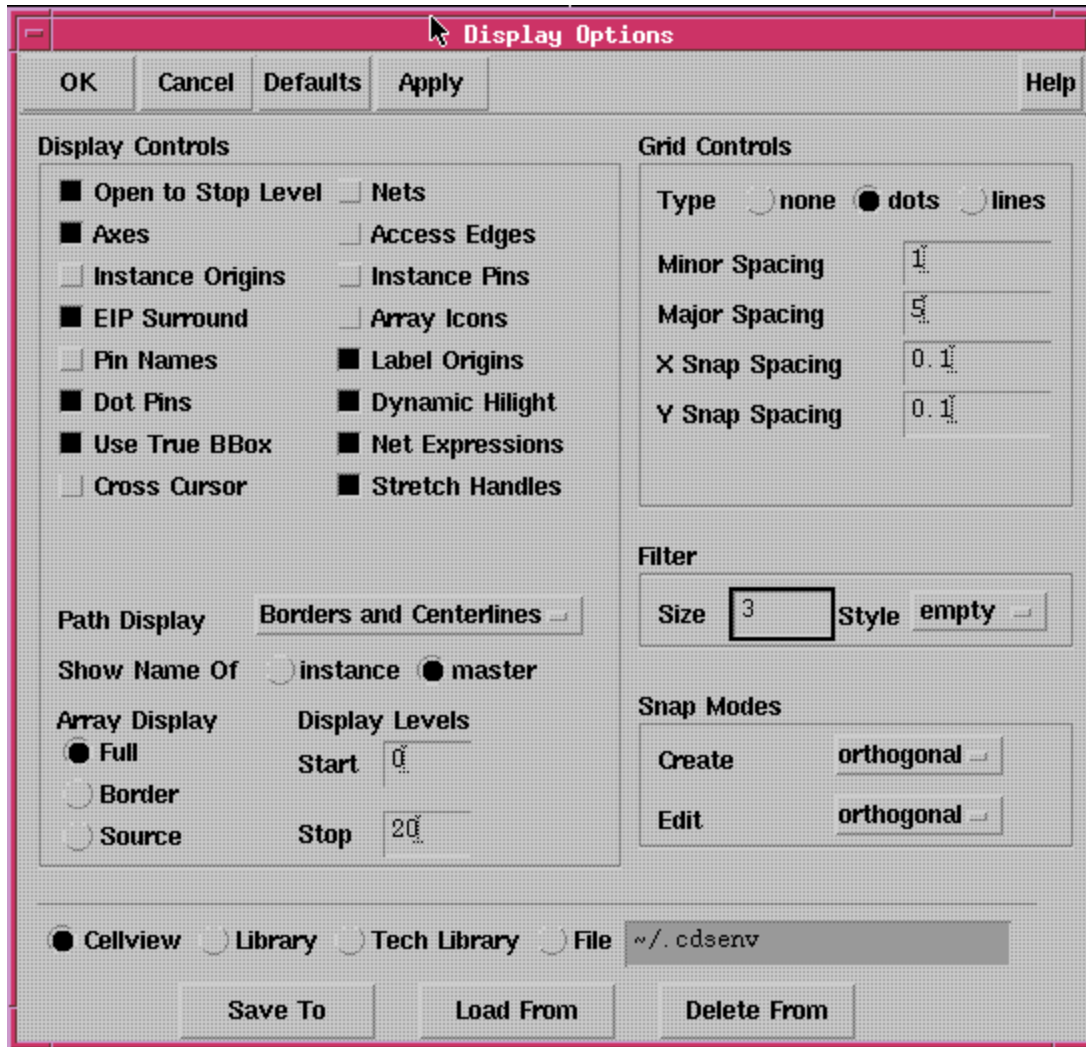


Fig. 3. Setting display options

- Now, to build an inverter, we will need nmos, ntap, pmos, ptap pcell.
- In *Layout Editing* window, select **Create --> Instance**.
  - Click Browse in *Create Instance* window.
  - The library browser window opens as shown in Fig. 4.
  - Select “NCSU\_TechLib\_tsmc02d” in the “library” column.
  - Select “nmos” in the “cell” column
  - Select “layout” in the “view” column
  - Press “Close”
- The create instance window will now appear as shown in Fig. 5.
- Change the width of the nmos cell according to what you have in the schematic of the inverter. Make sure you have the dimensions identical in both the schematic and the layout. Else, you will encounter LVS errors.
- Put nmos cell down in *Layout Editing* window like in Fig. 6.

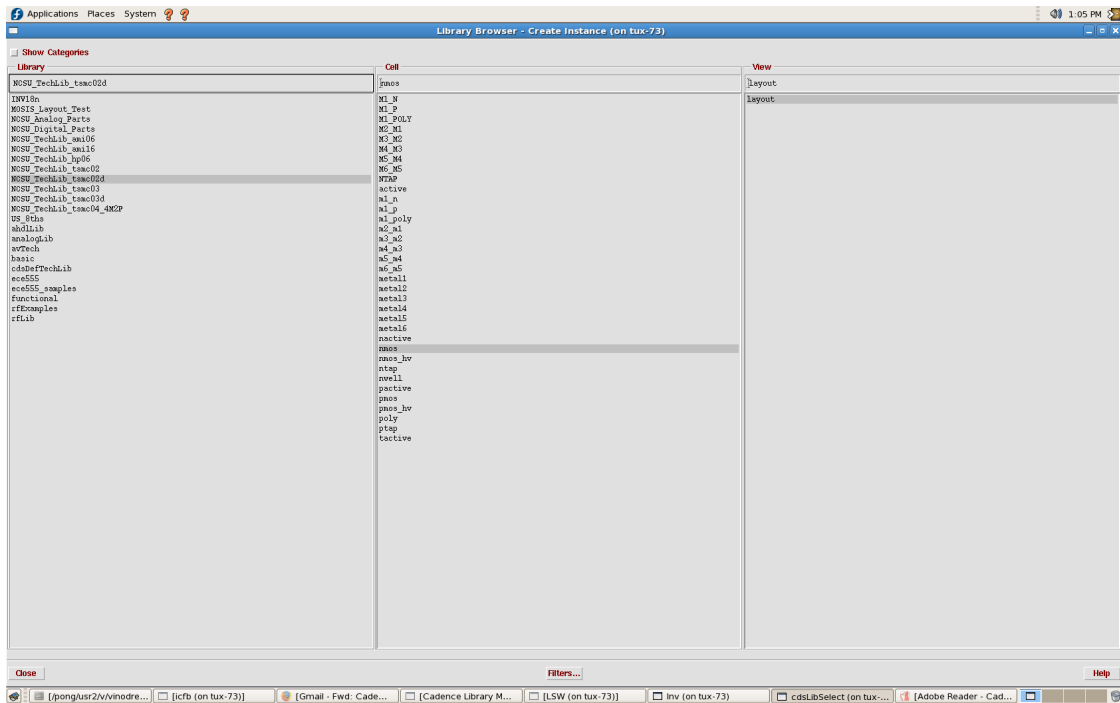


Fig. 4. Library Browser Window

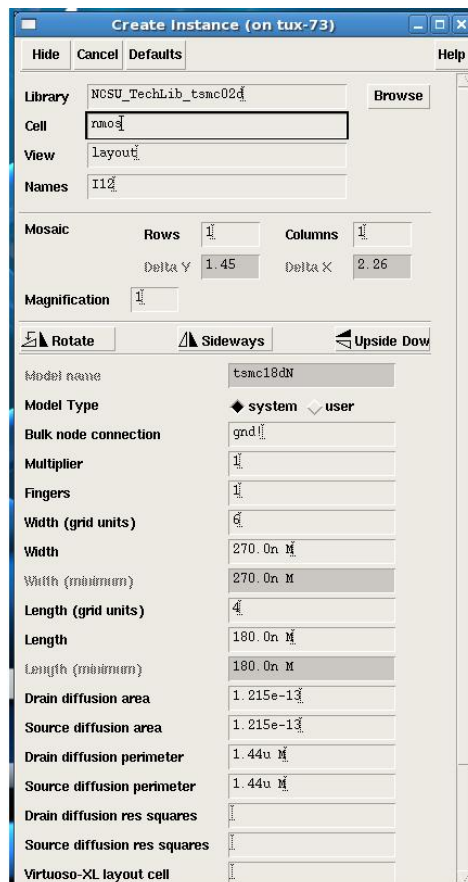


Fig. 5. Create Instance Window

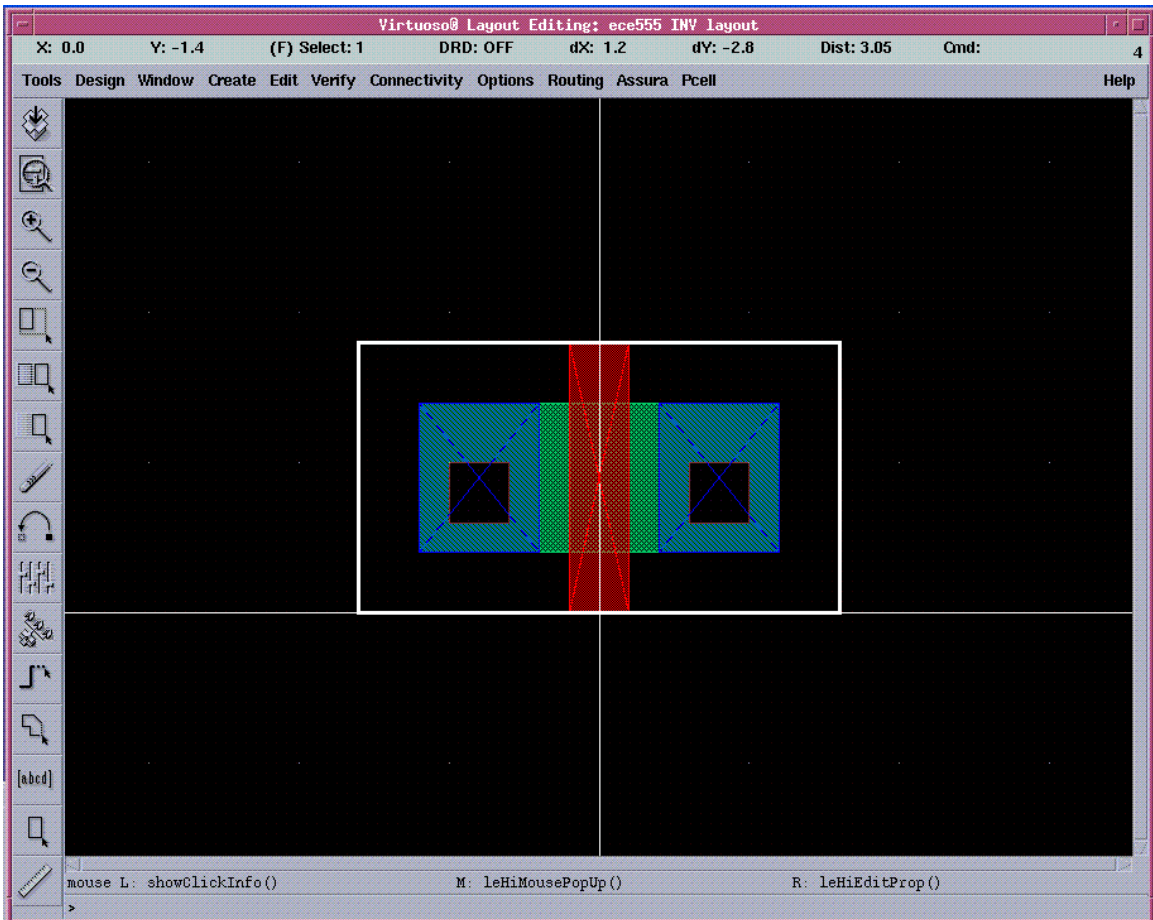


Fig. 6. Placing the nmos cell

- Repeat the steps for ntap, pmos, ptap and m1\_poly and move the cells around until it looks like Fig. 7.

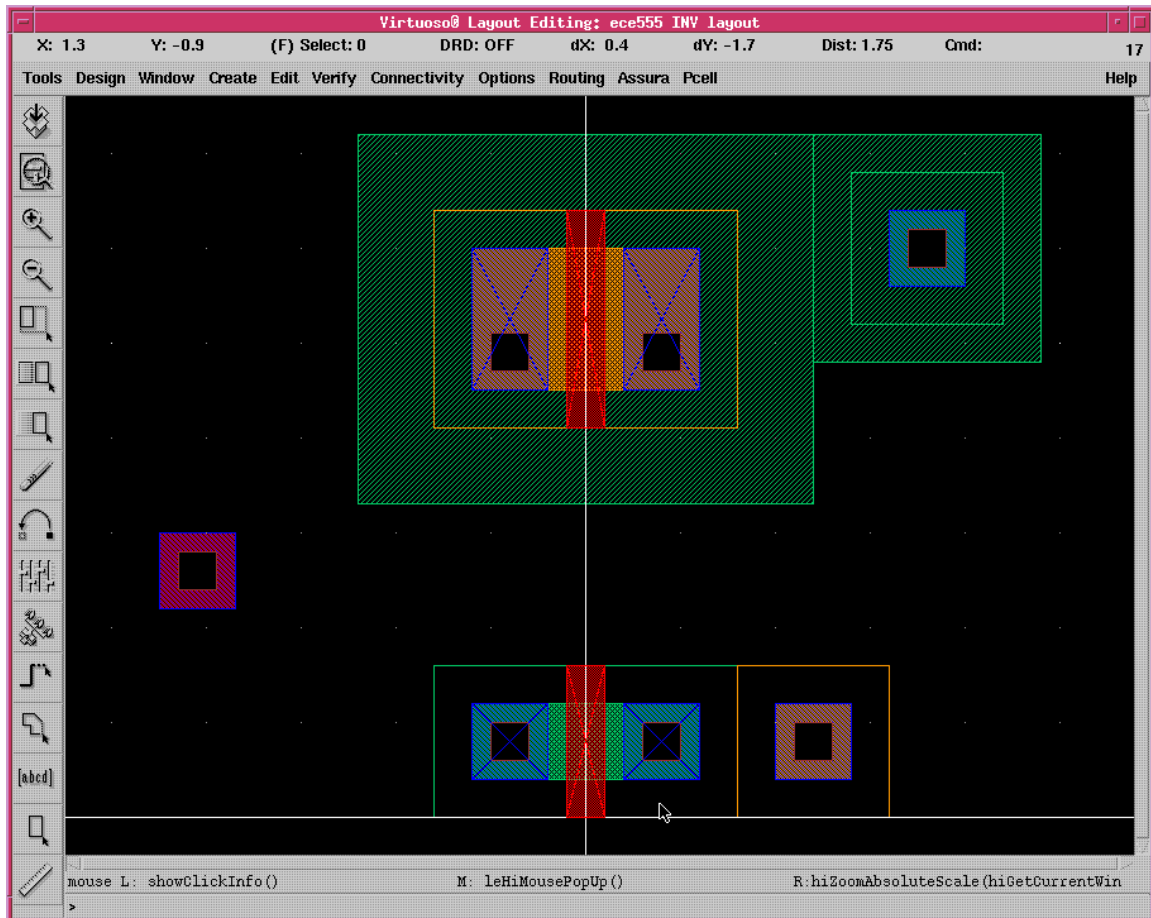


Fig. 7. Final placement of cells

- To draw power rails, click on metal 1(drw) in the *LSW* and go to **Create --> Rectangle** in the *Layout Editing* window.
- Left click once to indicate one corner of the rectangle and then move to another location and left click again to indicate the other diagonally opposite corner of the rectangle.
  - Draw the power rails as in Fig. 8.
  - You can use the object copy command to very efficiently here.
    - Draw just one power rail.
    - After drawing, select the rail. A white solid box appears around the selected object.
    - Press copy button on the left hand side of the Layout editing window.
    - Left Click on the selected object one more time to get hold of the copied instance of the object.
    - Position your cursor at the new location where you want to place the copied instance
    - Left click on the Layout editing window to place the copied instance.
- Add metal 1(drw) to ntap and source of the pmos for vdd!, as shown Fig. 9.

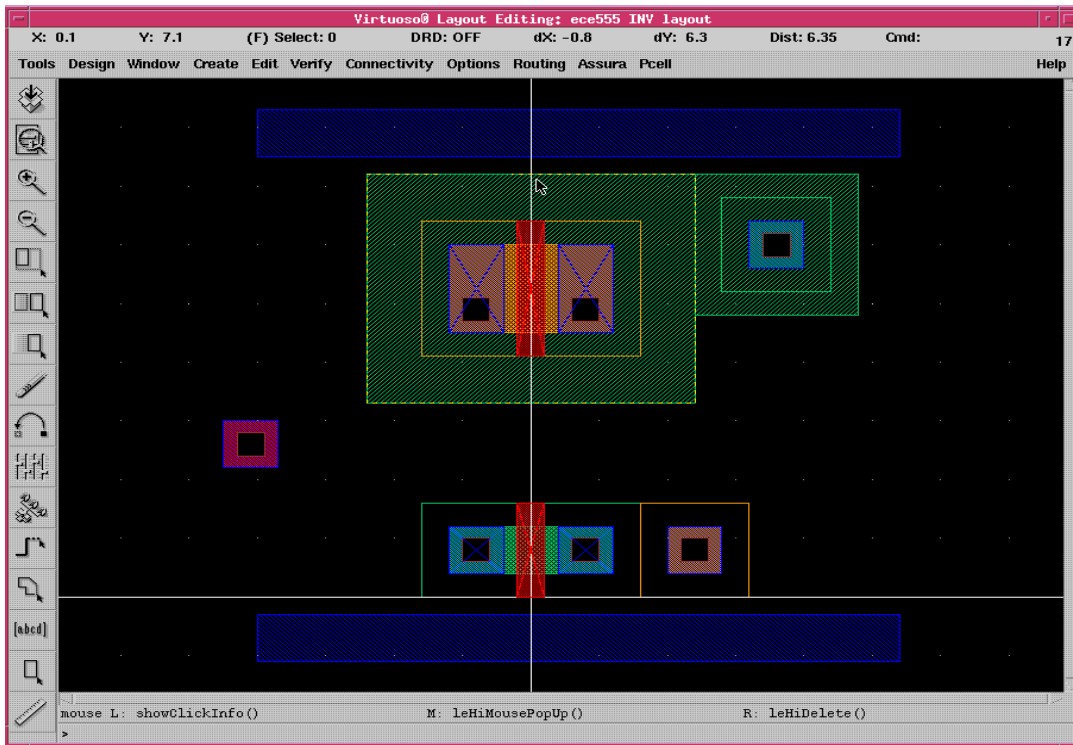


Fig. 8. Adding power rails

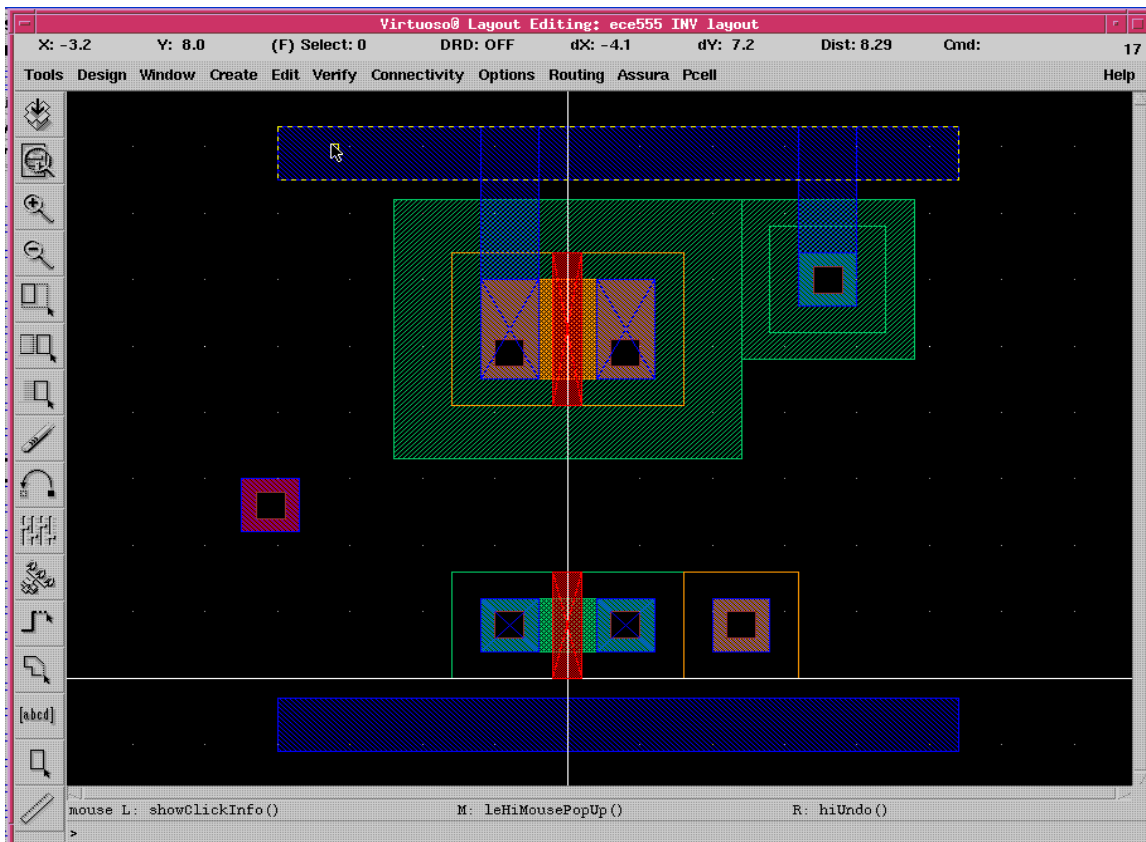


Fig. 9. Power connection to ntap and source of pmos

- Add metal 1(drw) to ptap and source of the nmos for gnd!, as in Fig. 10.

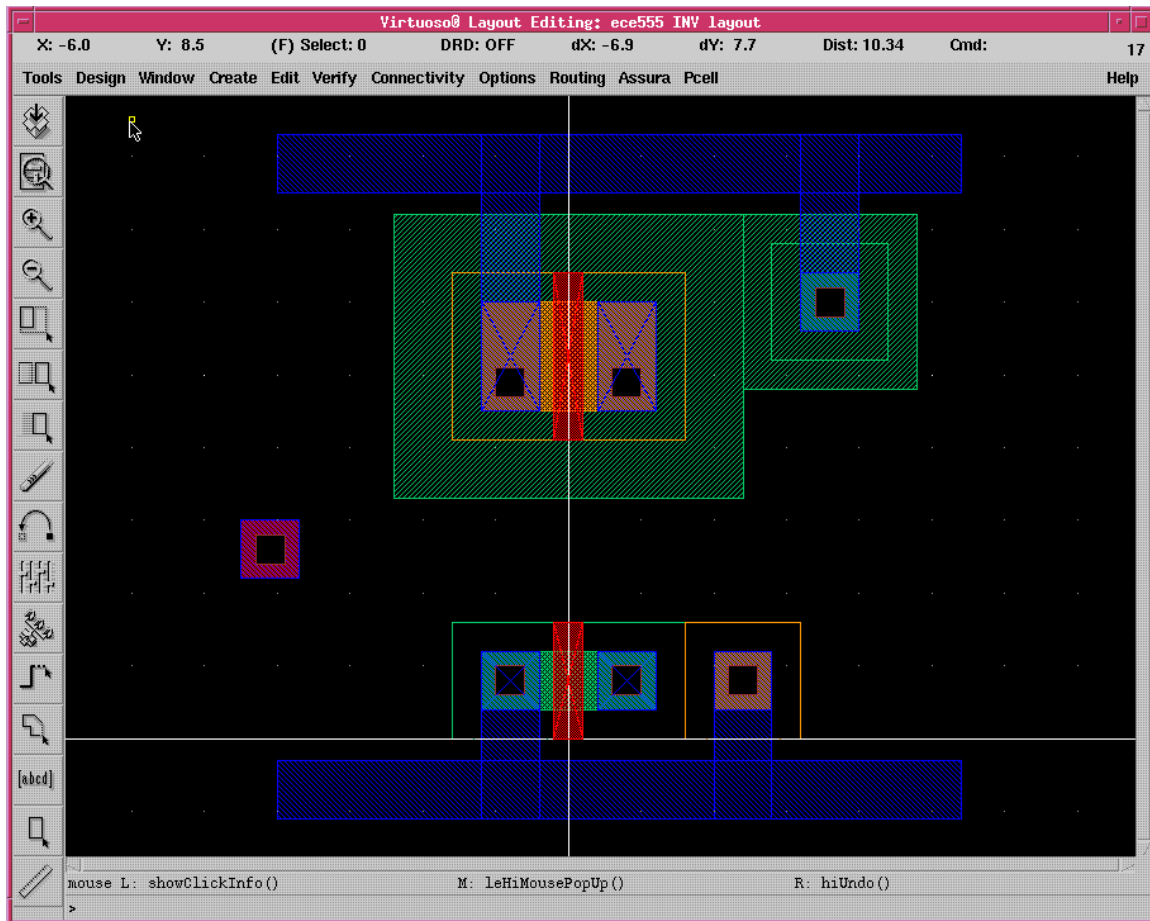


Fig. 10. Ground connection to ptap and source of nmos

- Connect the drains of nmos and pmos with metal 2(drw) for output as shown in Fig. 11.
- Now we need to connect the metal1 layer and the metal2 layer
  - As you instantiated the nmos, pmos etc, now instantiate a “m2\_m1” component from the “NCSU\_TechLib\_tsmc02d” library. This is a via.
  - Instantiate 2 copies of the “m2\_m1”.
  - Place one component at the drain of the pmos
  - Place another component at the drain of the nmos
  - Fig. 12 shows you the placement of the contacts.

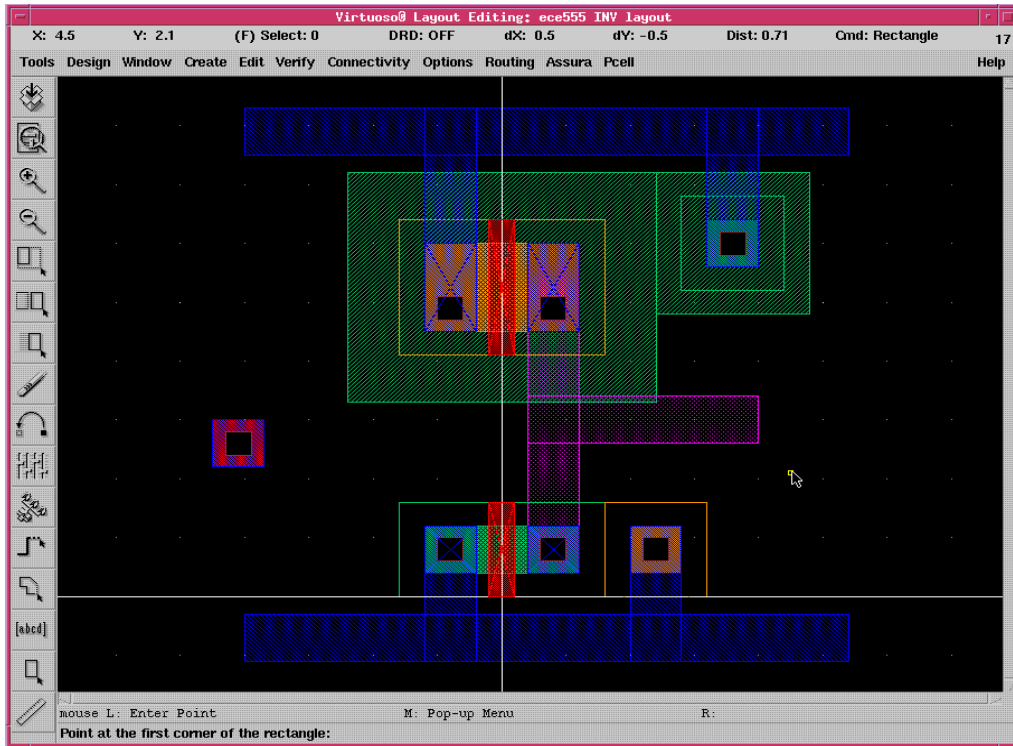


Fig. 11. Drain Connection using Metal 2

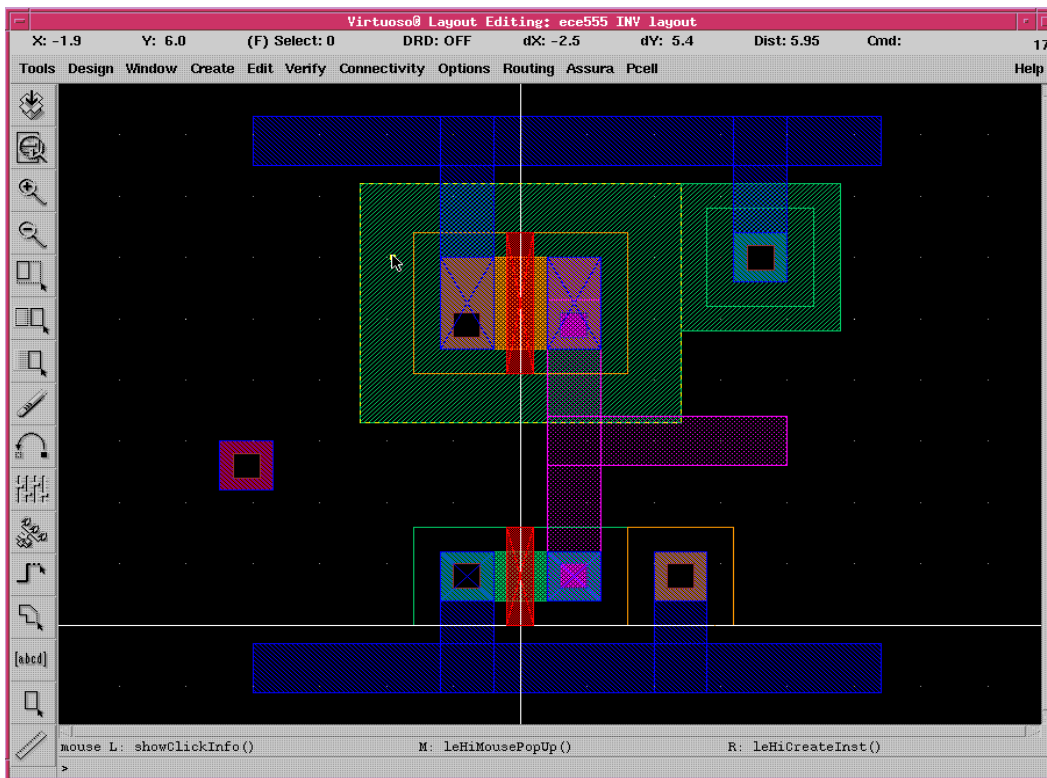


Fig. 12. Circuit after placing the contacts

- Connect the gates of the two transistors using a poly layer, as shown in Fig. 13.

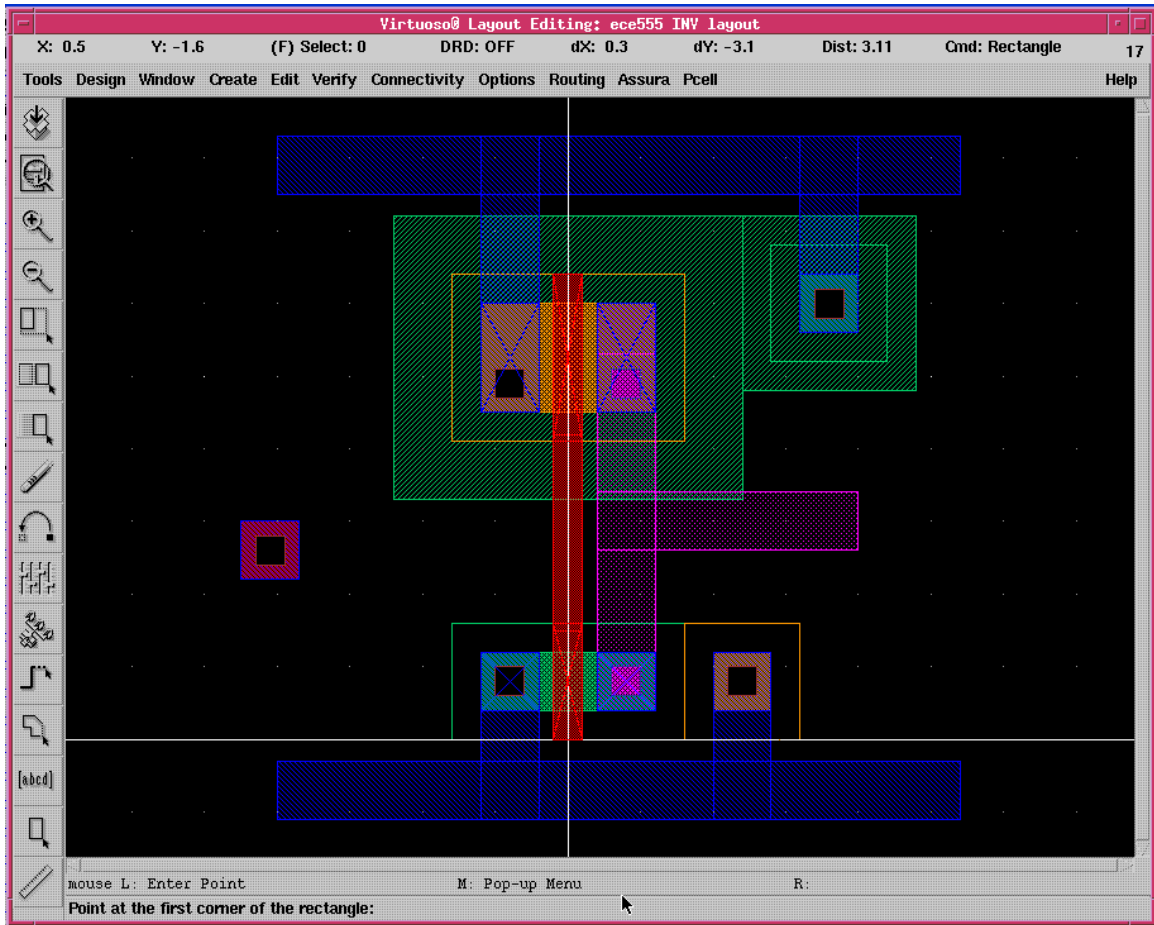


Fig. 13. Circuit after connecting the gates

- Now, add a poly connection to the m1\_poly via as Fig. 14. This is your completed layout without pins.

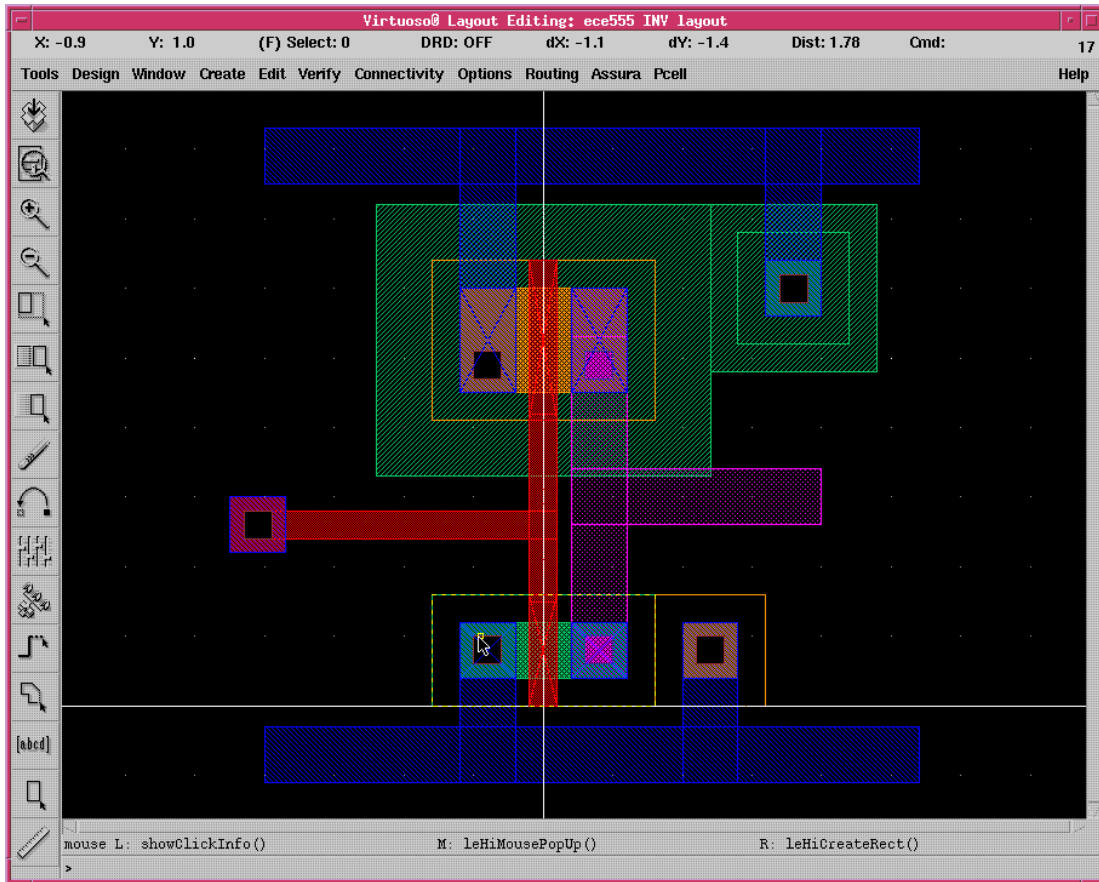


Fig. 14. Complete circuit without pins

- In order to simulate your extracted view of laid out inverter, you need to add four pins, vdd!, gnd!, A and Y.
  - The symbol "!" means that the variable name is global.
- Go to **Create --> Pin...** in the *Layout Editing* window and fill out like in Fig. 15.
- Place “vdd!” pin in the metal power bar on the pmos and “gnd!” pin in the metal power bar on the nmos. And, change I/O type in *Create Symbolic Pin* window to input for “in” and output for “out”. Then, place “out” in the metal region connecting drain of devices and “in” in the m1\_poly via. The completed layout of inverter should look like Fig. 16.
  - Make sure you select the appropriate pin type for each of the pin according to the metal layer in which the pin is placed.

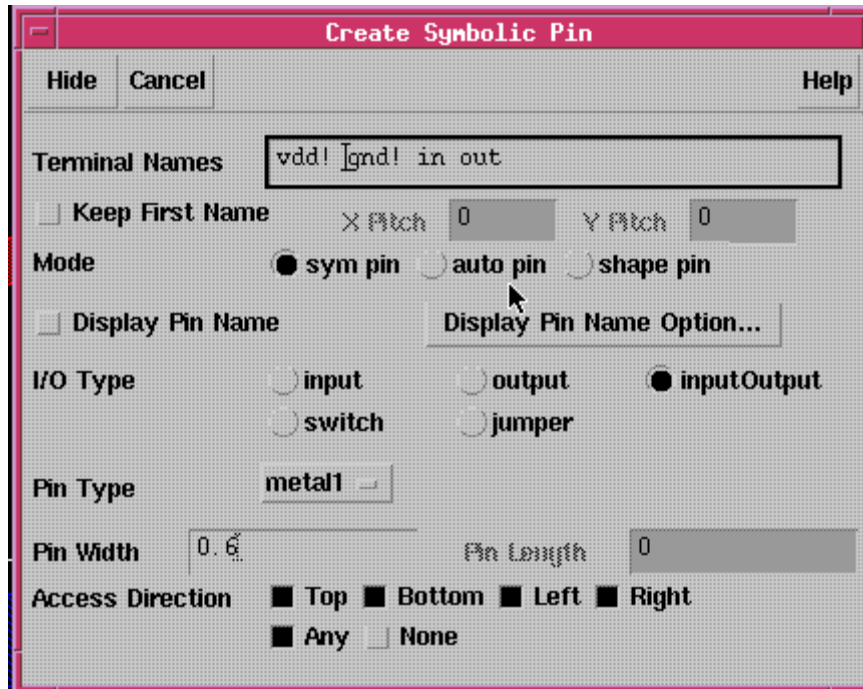


Fig. 15. Pin Creation

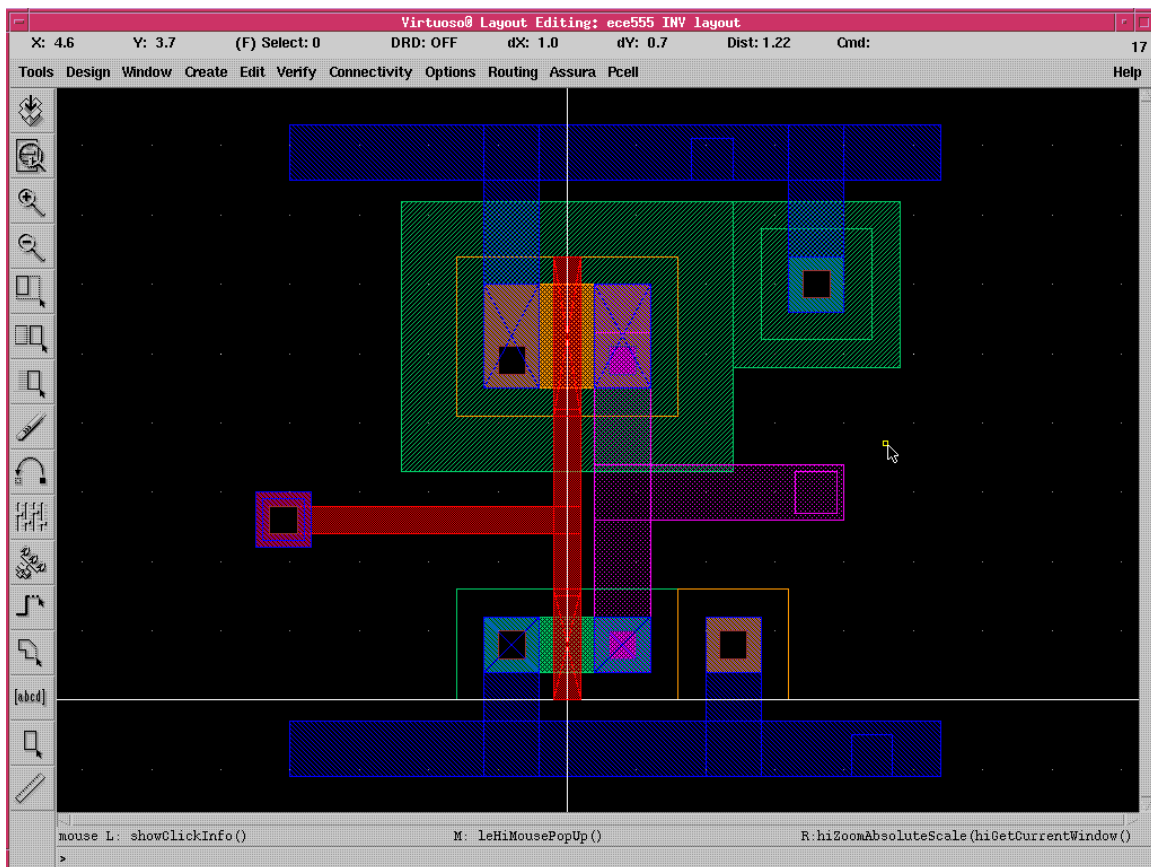


Fig. 16. Completed inverter layout

- Now, you are ready for DRC (Design Rule Checking).
- In *Layout Editing* window, select **Verify --> DRC...** Fig. 17 should appear. Just click OK

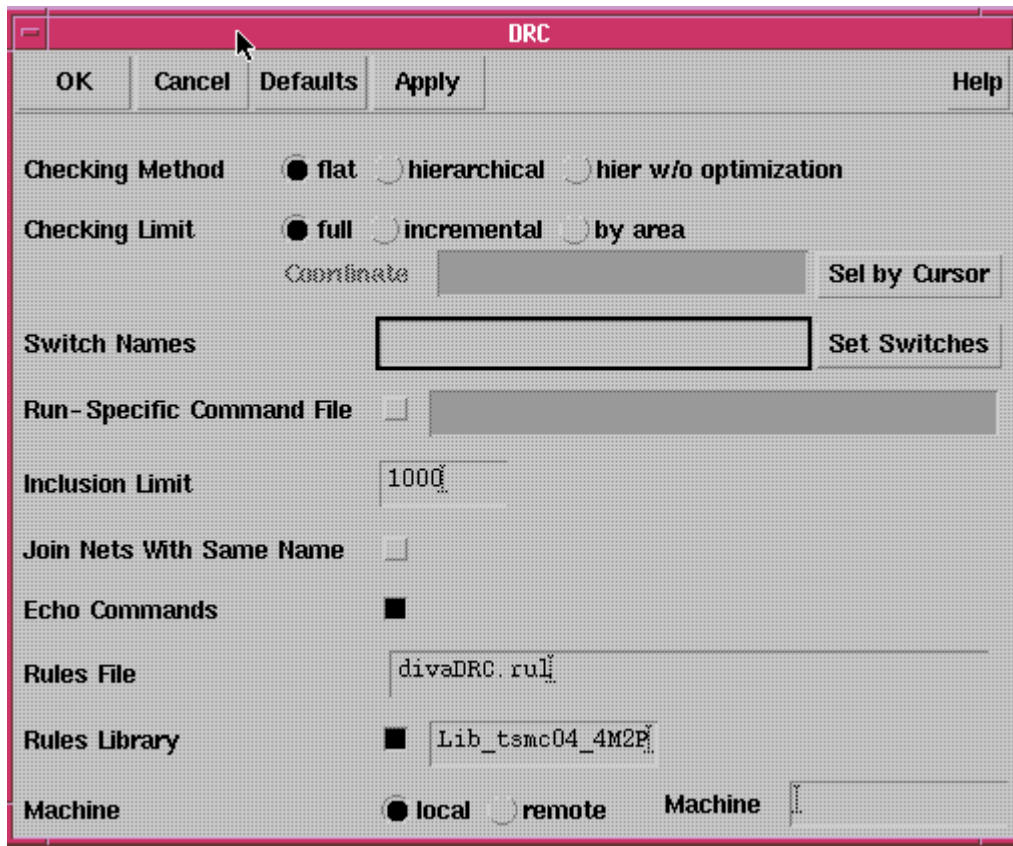


Fig. 17. Running DRC

- You can see those rules run across *CIW* very fast. Finally, you have *CIW* with no DRC error as in Fig. 18.
  - A DRC error will be manually generated and the procedure to remove it will be shown during the tutorial.

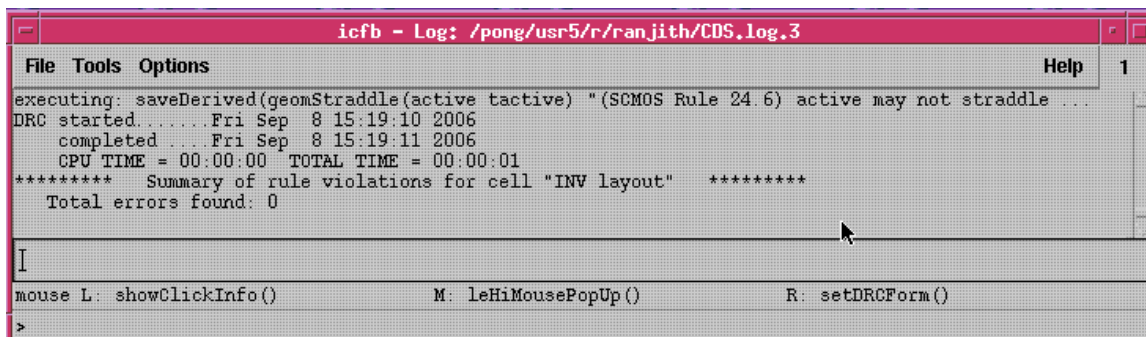


Fig.18. No DRC error

- Now that your inverter is laid out with no DRC errors, it is time to verify the function of this inverter.
- In *Layout Editing* window, select **Verify --> Extract...** Fig. 19 should appear.

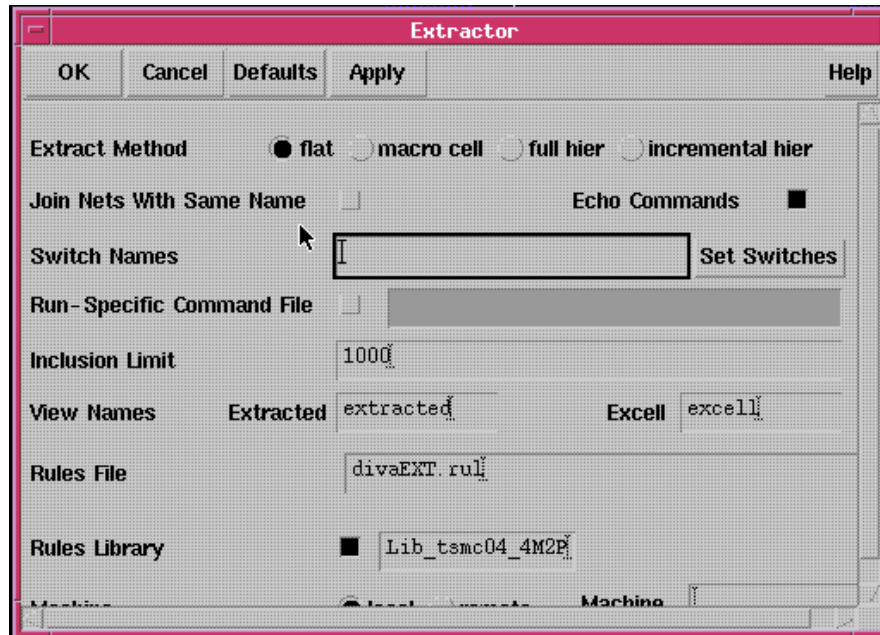


Fig.19. Extractor

- Select “Set Switches” and a window as shown in Fig 20 will appear.
- Select “Extract\_parasitic\_caps” and press OK
- Click OK to run Extractor. The *CIW* should give no error like in Fig. 21.

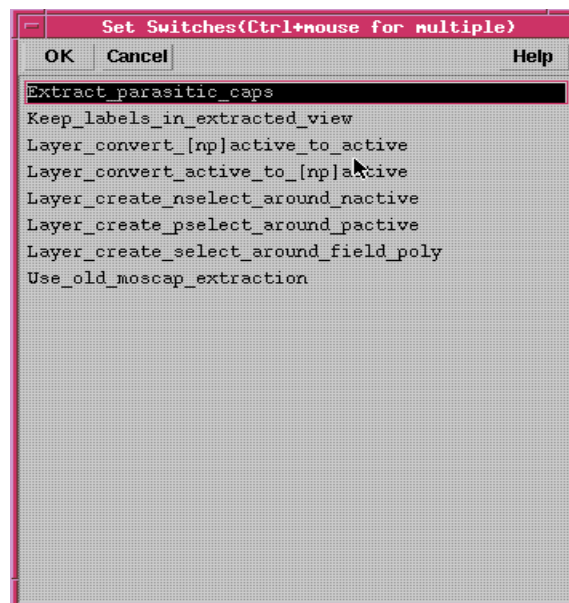


Fig.20. Set switches window

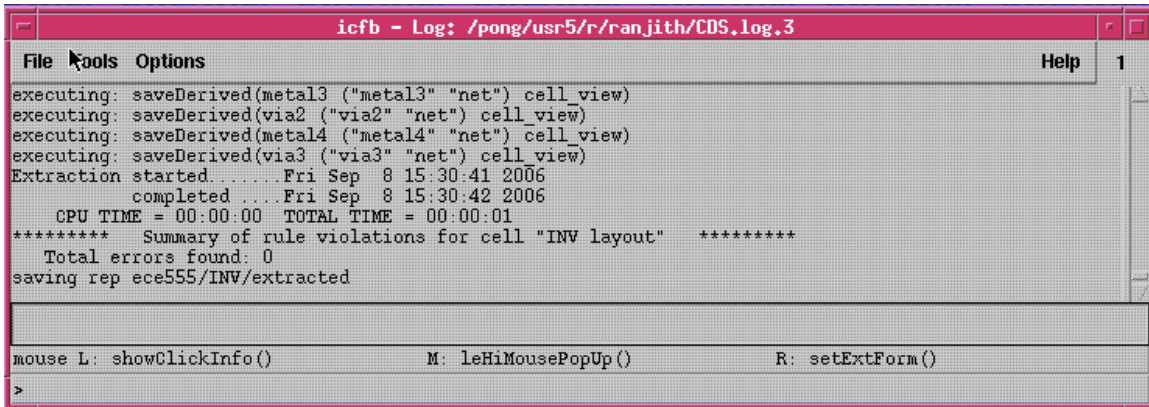


Fig.21. Extracted inverter with no error

- You are now going to perform LVS (Layout versus Schematic) using inverter you made earlier. An LVS makes sure that the circuit you laid out is equivalent to your schematic. You will also verify whether the post extraction simulation meets your specification with parasitic capacitance.
- In *Layout Editing* window, select **Verify --> LVS...** Fig. 22 should appear. Use the **Browse** button in *LVS window* to select that schematic and extracted view you are going to check for equivalence. You should have *LVS window* as Fig. 22. Just click run to start.

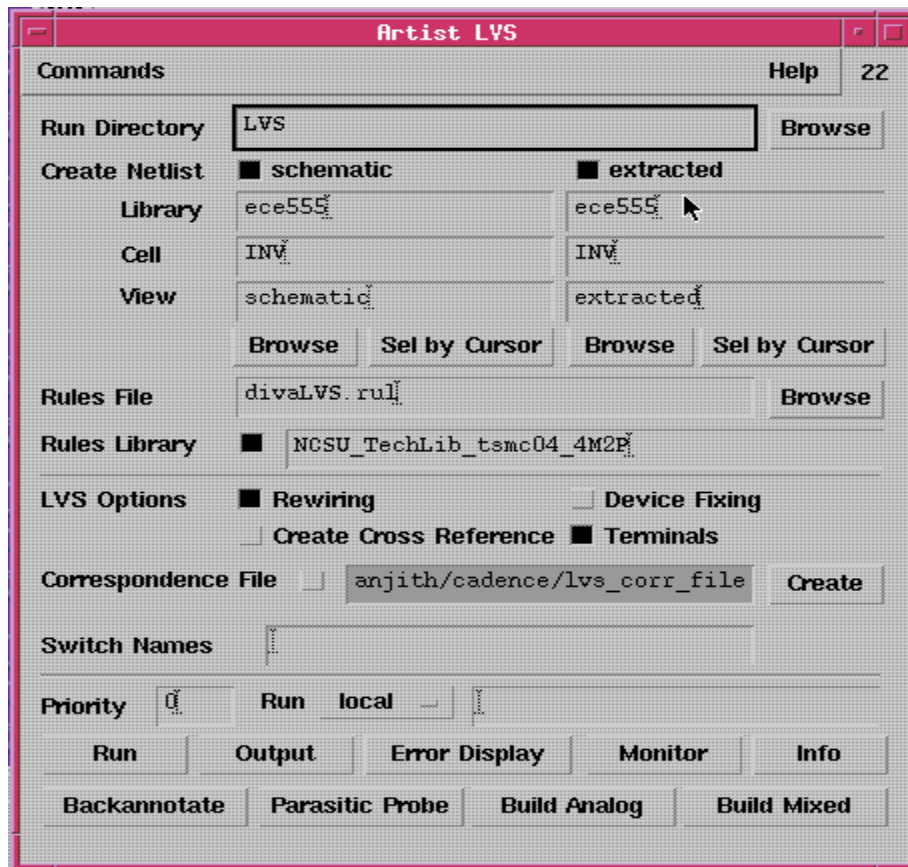


Fig. 22. Running LVS

- When the LVS check is successful, Fig. 23 should appear.

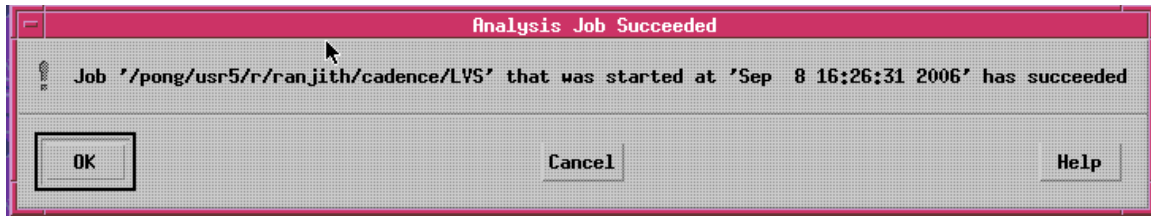


Fig. 23. Successful completion of an LVS check

- Press OK and then press the “OUTPUT” button. A window will pop up as shown in Fig. 24.
  - Your layout is perfect only if the output says “The net-lists match” and does not show any error in the probe section.

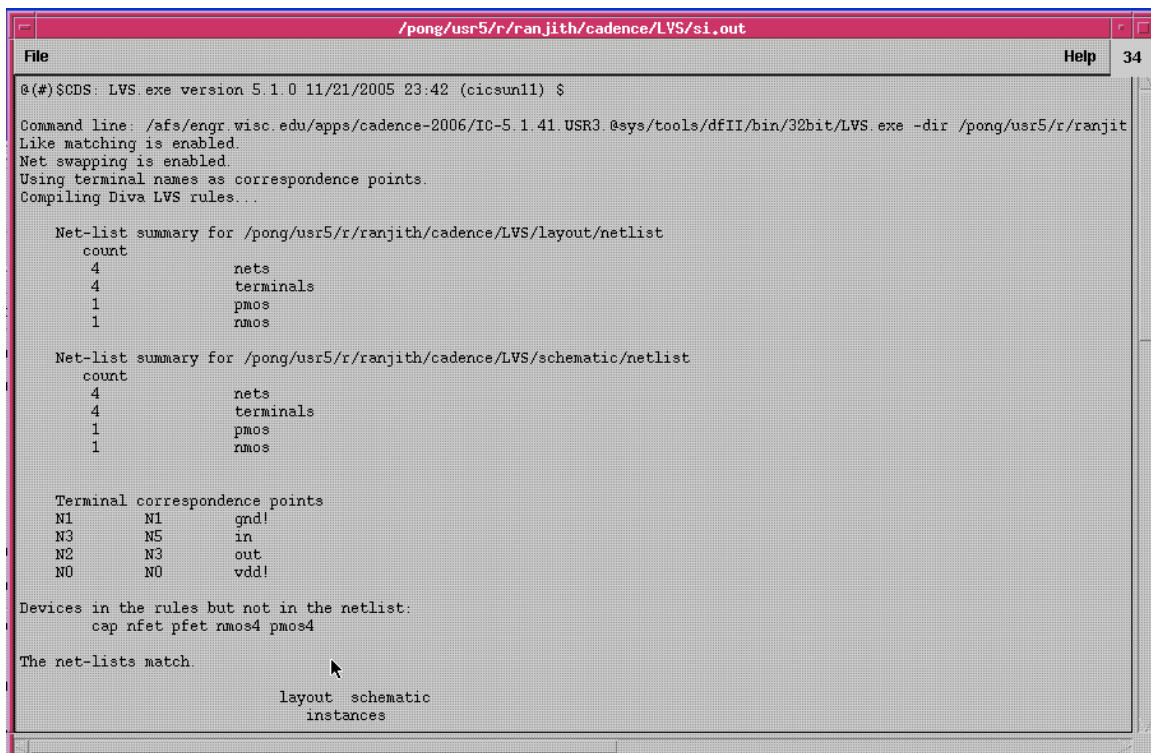


Fig. 24. LVS Output

- To find your extracted view of inverter, go to library manager and select extracted view. Your extracted view should be like Fig. 25. You can see two transistors and a parasitic capacitor which could affect the performance of your inverter.

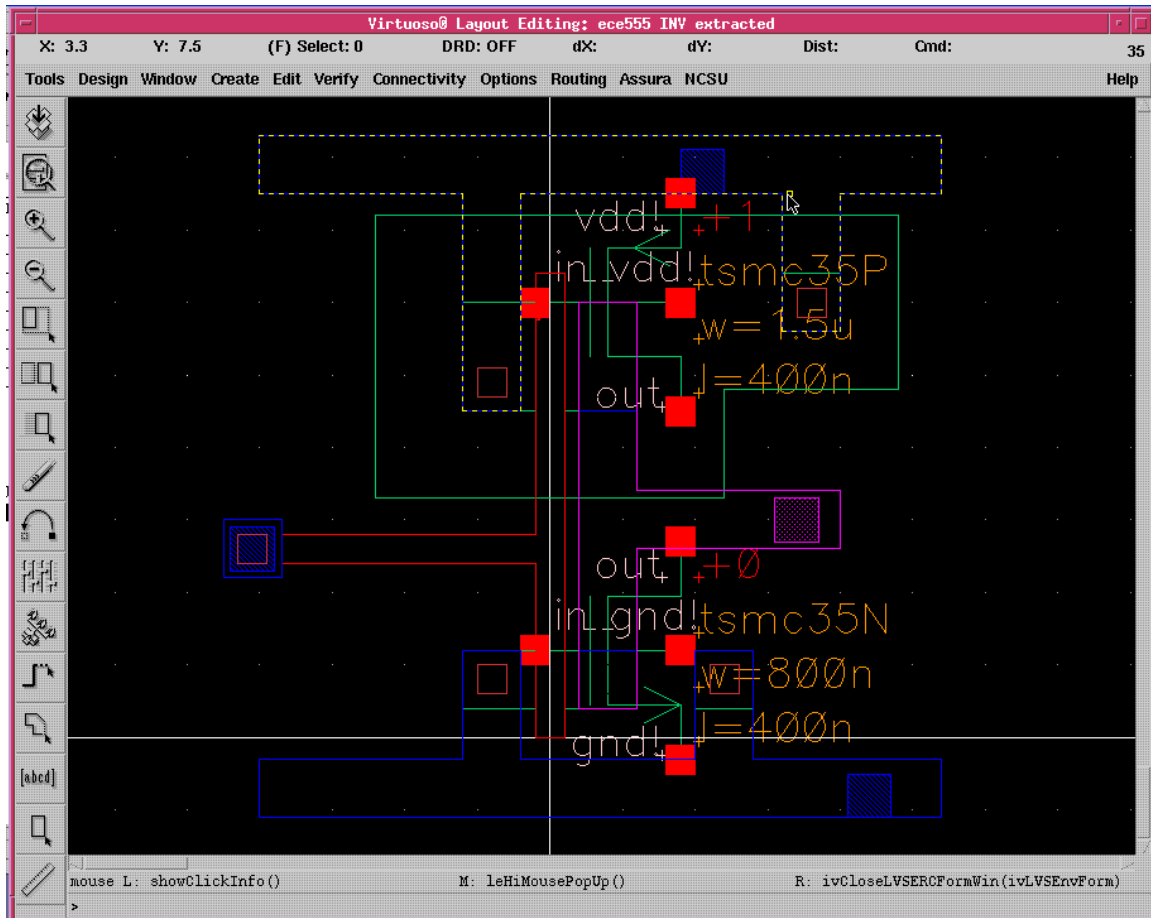


Fig. 25. Extracted view of the inverter

- In order to perform post extraction simulation,
  - Open up your extracted schematic and select **Tools -> Analog Environment** to get to the simulation environment as shown in Fig. 26.
  - Select **Setup --> Simulator/Directory/Host**.
    - A **Choosing Simulator/Directory/Host** window appears like Fig. 24. Make sure the simulator is set to **spectre**.
  - Select **Setup --> Environment**
    - Insert **extracted** view before the **spectre** in the **Switch View List** like in Fig. 27.
  - The other settings for the post-layout simulation are similar to the pre-layout simulation and hence are not repeated here.
    - Please refer Tutorial - I
  - Stimulus files are recommended for Post-Layout Simulations.
    - For how to write a stimulus file, please refer Tutorial - I
  - For propagation delay calculation
    - Please refer Tutorial-I

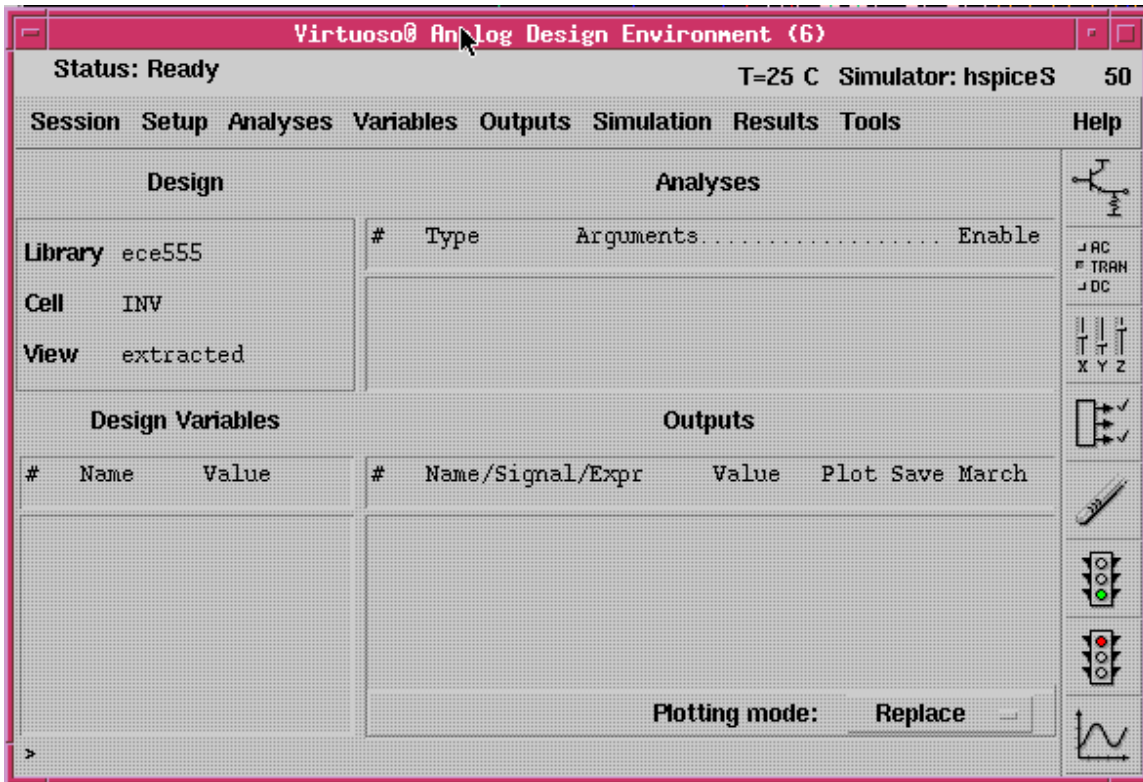


Fig. 26. Setting for post simulation

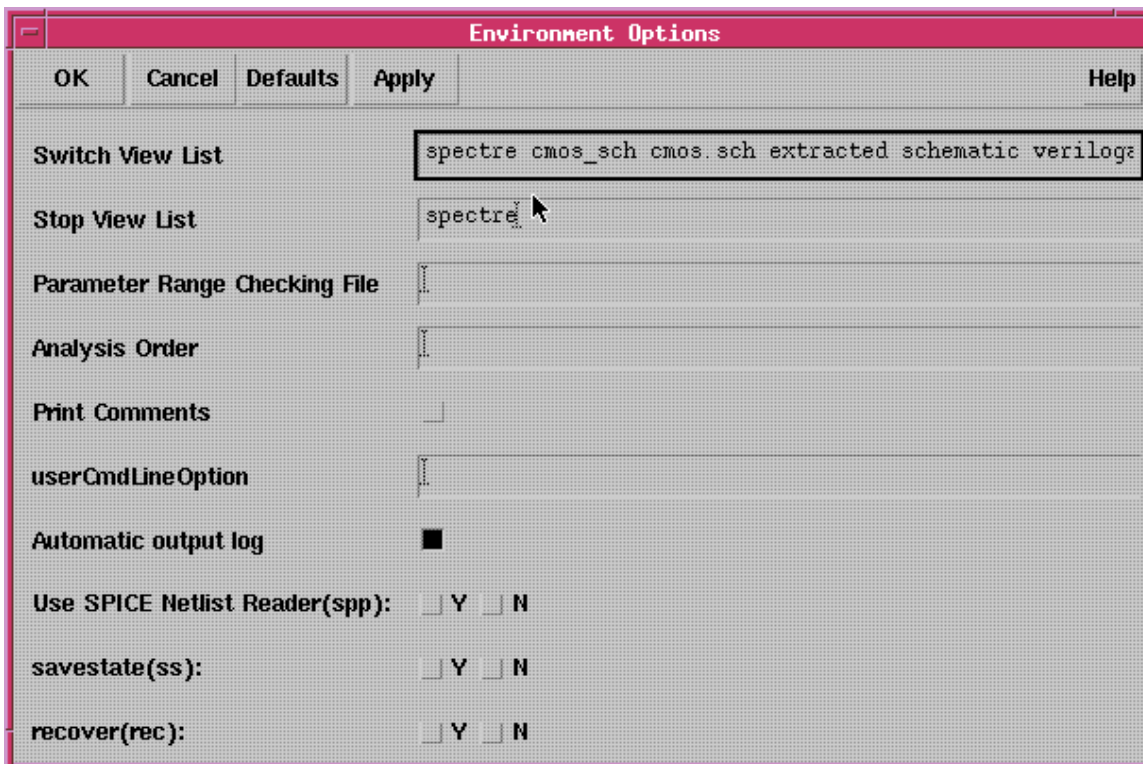


Fig. 27. Inserting extracted view