

**CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING  
COMPUTER SCIENCES DEPARTMENT  
UNIVERSITY OF WISCONSIN-MADISON**

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Midterm Examination 4  
In Class (50 minutes)  
Friday, December 14, 2007  
Weight: 15%

**CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.**

The exam is two-sided and has **TEN** pages, including two blank pages and a copy of the *Standard ASCII Table*, some *Trap Service Routines* description and the *LC-3 Instruction Set handout* on the final page (please feel free to detach this final page, but insert it into your exam when you turn it in).

Plan your time carefully, since some problems are longer than others.

NAME: \_\_\_\_\_

SECTION: \_\_\_\_\_

ID# \_\_\_\_\_

<b>Problem Number</b>	<b>Maximum Points</b>	<b>Points Awarded</b>
1	4	
2	2	
3	7	
4	8	
5	7	
6	2	
Total	30	

**Problem 1 (4 points): Short Answers**

a. What is the problem with using the string NOT as a label in an LC-3 assembly language program?

b. What single instruction is equivalent to the following two LC-3 instructions?

```
LEA R7, #1  
JMP R2, #0
```

c. The LC-3 assembly process is done in two complete passes through the entire assembly language program. What is the objective of the first pass?

d. What is the purpose of .ORIG pseudo-op?

**Problem 2 (2 points): Memory-Mapped I/O**

Suppose an ISA has a 16-bit address space. All addresses wherein bits[15:12] = 1111 are allocated to I/O device registers.

a. What is the minimum address of I/O device registers?

b. What is the maximum address of I/O device registers?

**Problem 3 (7 points): Two-Pass Assembly Process**

An assembly language LC-3 program is given below:

```
1      .ORIG x3000
2  ONE LD   R2, A
3      ADD  R1, R1, R2
4  TWO LD   R2, B
5      ADD  R1, R1, R2
6      ST   R1, SUM
7      TRAP x25
8  A    .FILL x1111
9  B    .FILL x2222
10 C    .FILL x3333
11     .END
```

a. Fill in the symbol table for the program:

Symbol	Address
ONE	x3000

b. Assuming that both passes of the assembler were to execute, write the binary word (machine language instruction) that would be generated by the assembler for the first instruction of the program.

c. The programmer intended the program to add the values stored in memory locations A and B, and store the result into memory. There are two errors in the code. For each, describe the error and indicate whether it will be detected at assembly time or at run time.

#### Problem 4 (8 points): Trap Routines and Save/Restore Problem

Suppose we define a new service routine starting at memory location x4200. This routine reads in a character and echoes it to the screen. Suppose memory location x0062 contains the value x4200. The service routine is shown below.

```
01          .ORIG x4200
02          ST   R0,  SAVERA
03          ST   __,  SAVERB
04          GETC
05          OUT
06          LD   R0,  SAVERA
07          LD   __,  SAVERB
08          RET
09 SAVERA   .FILL x0000
10 SAVERB   .FILL x0000
```

- a. Fill the blanks in the above program.
- b. Identify the instruction that will invoke this routine.
- c. Line 10 is the RET instruction, will a BR (Unconditional branch) instruction work instead? Why or why not?
- d. What do instructions in line 02 and 06 do? Will the service routine work without these two lines? Why or why not?



- c. Memory mapped and polling
- d. Special opcode for I/O and polling

**Problem 6 (2 points): Professional Ethics**

Regarding the assigned reading "RFID Inside" on RFID implants, do you support RFID implants? Why or why not? Give two different reasons to support your position.

**Scratch Sheet 1 (in case you need additional space for some of your answers)**



## ASCII Table

Character	Hex	Character	Hex	Character	Hex	Character	Hex
nul	00	sp	20	@	40	`	60
soh	01	!	21	A	41	a	61
stx	02	"	22	B	42	b	62
etx	03	#	23	C	43	c	63
eot	04	\$	24	D	44	d	64
enq	05	%	25	E	45	e	65
ack	06	&	26	F	46	f	66
bel	07	'	27	G	47	g	67
bs	08	(	28	H	48	h	68
ht	09	)	29	I	49	i	69
lf	0A	*	2A	J	4A	j	6A
vt	0B	+	2B	K	4B	k	6B
ff	0C	,	2C	L	4C	l	6C
cr	0D	-	2D	M	4D	m	6D
so	0E	.	2E	N	4E	n	6E
si	0F	/	2F	O	4F	o	6F
dle	10	0	30	P	50	p	70
dc1	11	1	31	Q	51	q	71
dc2	12	2	32	R	52	r	72
dc3	13	3	33	S	53	s	73
dc4	14	4	34	T	54	t	74
nak	15	5	35	U	55	u	75
syn	16	6	36	V	56	v	76
etb	17	7	37	W	57	w	77
can	18	8	38	X	58	x	78
em	19	9	39	Y	59	y	79
sub	1A	:	3A	Z	5A	z	7A
esc	1B	;	3B	[	5B	{	7B
fs	1C	<	3C	\	5C		7C
gs	1D	=	3D	]	5D	}	7D
rs	1E	>	3E	^	5E	~	7E
us	1F	?	3F	_	5F	del	7F

## Trap Service Routines

Trap Vector	Assembler Name	Description
x20	GETC	Read a single character from the keyboard. The Character is not echoed onto the console. Its ASCII code is copied into R0. The high eight bits of R0 are cleared.
x21	OUT	Write a character in R0[7:0] to the console display.
...	...	...
x25	HALT	Halt execution and print a message on the console.

# LC-3 Instruction Set (Entered by Mark D. Hill on 03/14/2007; last update 03/15/2007)

PC': incremented PC. setcc(): set condition codes N, Z, and P. mem[A]:memory contents at address A.  
 SEXT(immediate): sign-extend immediate to 16 bits. ZEXT(immediate): zero-extend immediate to 16 bits.  
 Page 2 has an ASCII character table.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ADD DR, SR1, SR2 ; Addition
0	0	0	0	1	DR		SR1	0	0	0	0		SR2			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 + SR2 also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ADD DR, SR1, imm5 ; Addition with Immediate
0	0	0	0	1	DR		SR1	1		imm5						
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 + SEXT(imm5) also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																AND DR, SR1, SR2 ; Bit-wise AND
0	1	0	0	1	DR		SR1	0	0	0	0		SR2			
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 AND SR2 also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																AND DR, SR1, imm5 ; Bit-wise AND with Immediate
0	1	0	0	1	DR		SR1	1		imm5						
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← SR1 AND SEXT(imm5) also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																BRx, label (where x = {n,z,p,zp,np,nz,nzp}) ; Branch
0	0	0	0	0	n	z	p									PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																GO ← ((n and N) OR (z AND Z) OR (p AND P)) if (GO is true) then PC ← PC' + SEXT(PCOffset9)
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JMP BaseR ; Jump
1	1	0	0	0	0	0	0		BaseR	0	0	0	0	0	0	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																PC ← BaseR
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JSR label ; Jump to Subroutine
0	1	0	0	0	1											PCOffset11
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																R7 ← PC', PC ← PC' + SEXT(PCOffset11)
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																JSRR BaseR ; Jump to Subroutine in Register
0	1	0	0	0	0	0	0		BaseR	0	0	0	0	0	0	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																temp ← PC', PC ← BaseR, R7 ← temp
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LD DR, label ; Load PC-Relative
0	0	1	0		DR											PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[PC' + SEXT(PCOffset9)] also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LDI DR, label ; Load Indirect
1	0	1	0		DR											PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[mem[PC' + SEXT(PCOffset9)]] also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LDR DR, BaseR, offset6 ; Load Base+Offset
0	1	1	0		DR		BaseR									offset6
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← mem[BaseR + SEXT(offset6)] also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																LEA, DR, label ; Load Effective Address
1	1	1	0		DR											PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← PC' + SEXT(PCOffset9) also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																NOT DR, SR ; Bit-wise Complement
1	0	0	0	1		DR		SR	1	1	1	1	1	1	1	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																DR ← NOT(SR) also setcc()
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																RET ; Return from Subroutine
1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																PC ← R7
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																RTI ; Return from Interrupt
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																See textbook (2 <sup>nd</sup> Ed. page 537).
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																ST SR, label ; Store PC-Relative
0	0	1	1		SR											PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[PC' + SEXT(PCOffset9)] ← SR
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																STI, SR, label ; Store Indirect
1	0	1	1		SR											PCOffset9
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[mem[PC' + SEXT(PCOffset9)]] ← SR
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																STR SR, BaseR, offset6 ; Store Base+Offset
0	1	1	1		SR		BaseR									offset6
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																mem[BaseR + SEXT(offset6)] ← SR
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																TRAP ; System Call
1	1	1	1	0	0	0	0									trapvect8
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																R7 ← PC', PC ← mem[ZEXT(trapvect8)]
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																; Unused Opcode
1	1	0	1													
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+																Initiate illegal opcode exception