CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN – MADISON

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Midterm Examination 2

In Class (50 minutes)

Friday, October 23, 2009

Weight: 15%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam has **four** two-sided pages.

Plan your time carefully, since some problems are longer than others.

NAME:_____

SECTION:_____

ID#:_____

Problem Number	Maximum Points	Actual Points
1	3	
2	4	
3	4	
4	3	
5	4	
6	3	
7	2	
8	3	
9	4	
Total	30	

Problem 1 (3 points)

Write the Boolean expression corresponding to the following truth table. You need not simplify the expression.
e.g. Z = __ __ __ + __ __ __ + ...

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Z = (~A & ~B & ~C) | (~A & ~B & C) | (A & B & ~C)

Problem 2 (4 points)

Suppose a 32-bit instruction takes the following format:

OPCODE	SR	DR	IMM

If there are 350 opcodes and 32 registers:

a) What is the minimum number of bits required to represent the OPCODE?

350 ≤ 512 = 2^9 => 9 bits

b) What are the minimum number of bits required to represent source register (SR) and destination register (DR)?

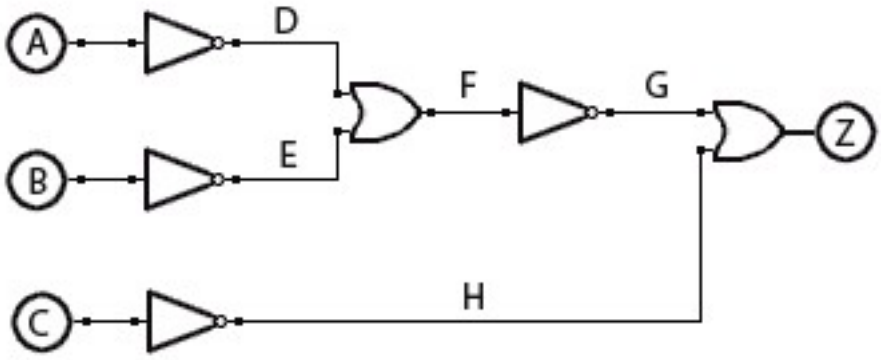
32 = 2^5 => 5 bits

c) (2 points) What is the range of values that can be represented by the immediate (IMM)? Assume IMM is a two's complement value.

32 – (9 + 5 + 5) = 13
-2^12 ≤ IMM ≤ 2^12 – 1

Problem 3 (4 points)

The figure below shows a combinational logic circuit. A, B, and C are the inputs to the circuit, Z is the output, and D, E, F, G, H are internal wires.



a) What is the output Z when A = 1, B = 0, C = 1? Explain by identifying the values of internal wires.

D = 0
E = 1
F = 1
G = 0
H = 0

Z = 0

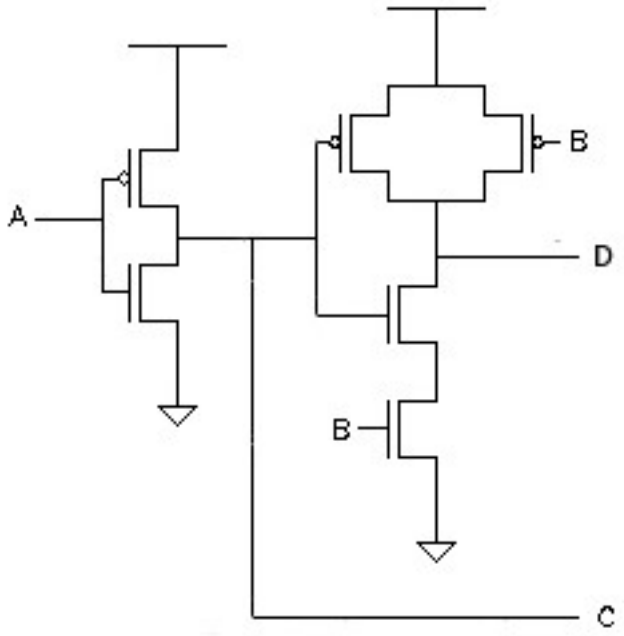
b) What is the output Z when C = 0? Explain.

C = 0
H = 1

Z is always 1.

Problem 4 (3 points)

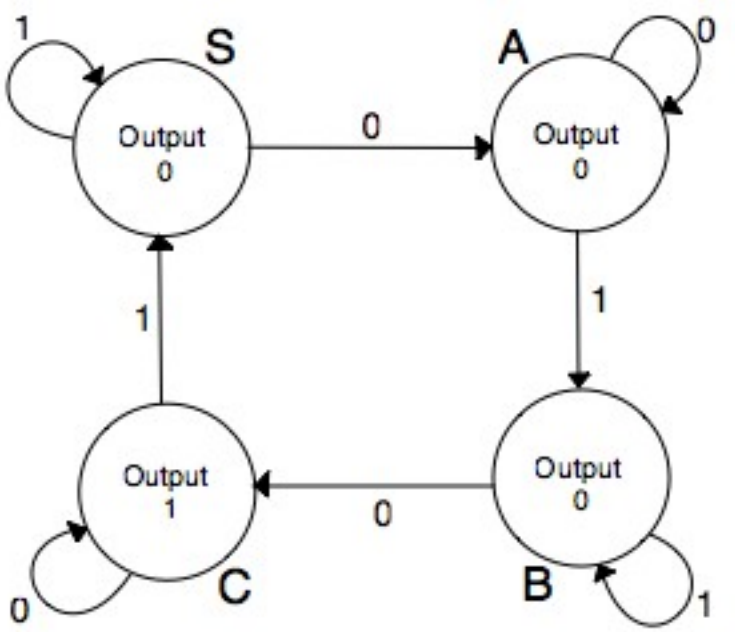
Fill in the truth table for C and D for the following transistor level circuit. Note that the two wires labeled B are assumed to be connected to each other.



A	B	C	D
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1

Problem 5 (4 points)

The figure below is a finite state machine (FSM) diagram, where the start state is S. Complete the questions according to the behavior of this machine.



a) If an input sequence is: 100110, write the state changes (eg. S → __ → __ → ...).

S → S → A → A → B → B → C

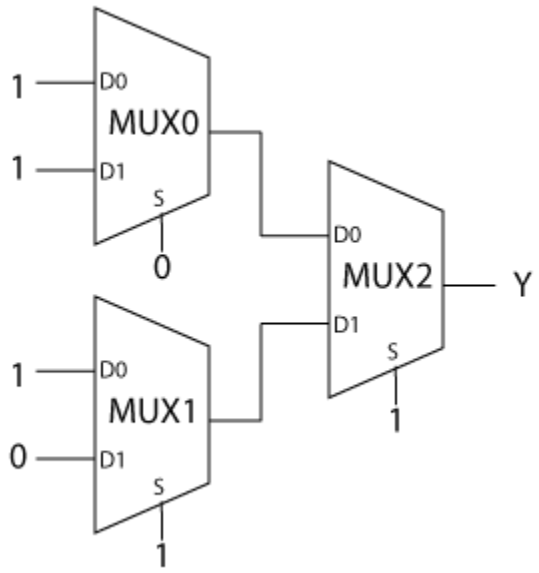
b) For the same input sequence 100110, what is the output sequence?

0 0 0 0 0 1

c) (2 points) Assume the current state is A, what input sequence will put the FSM back to state S?

1 0 1

Problem 6 (3 points)



The figure above is a circuit with three 2-to-1 multiplexers. What is the output Y? Explain.

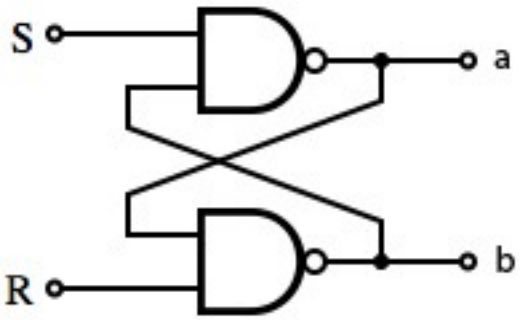
MUX0 outputs D0 value 1.
MUX1 outputs D1 value 0.
MUX2 selects D1 (MUX1's output), thus Y = 0.

Problem 7 (2 points)

A load to a memory uses a 6-bit address A[5:0] to obtain a 11-bit value V[10:0]. What is the total number of bits that can be stored in all of the memory?

2^6 * 11 = 64 * 11 = 704

Problem 8 (3 points)



a) For this R-S latch, what are the values of a and b if S = 1, and R = 0?

a = 0
b = 1

b) Then, R changes to 1 (now S = 1, R = 1). What are the values of a and b?

a = 0
b = 1

c) Then, S changes to 0 (now S = 0, R = 1). What are the values of a and b?

a = 1
b = 0

Problem 9 (4 points)

Circle the correct answer.

a) A 4-state finite state machine can be implemented using 2 D-latches. [True / **False**]

b) The ADD instruction leaves the program counter unchanged. [True / **False**]

c) The instruction register holds the address of the instruction to be executed next. [True / **False**]

d) The LDR (load) instruction writes to a register. [**True** / False]