

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN – MADISON

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Midterm Examination 2

In Class (50 minutes)

Friday, October 23, 2009

Weight: 15%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam has **four** two-sided pages.

Plan your time carefully, since some problems are longer than others.

NAME: _____

SECTION: _____

ID#: _____

Problem Number	Maximum Points	Actual Points
1	3	
2	4	
3	4	
4	3	
5	4	
6	3	
7	2	
8	3	
9	4	
Total	30	

Problem 1 (3 points)

Write the Boolean expression corresponding to the following truth table. You need not simplify the expression.

e.g. $Z = _ _ _ + _ _ _ + \dots$

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$$Z = (\sim A \ \& \ \sim B \ \& \ C) \mid (\sim A \ \& \ B \ \& \ C) \mid (A \ \& \ \sim B \ \& \ C)$$

Problem 2 (4 points)

Suppose a 32-bit instruction takes the following format:

OPCODE	SR	DR	IMM
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If there are 550 opcodes and 32 registers:

a) What is the minimum number of bits required to represent the OPCODE?

$$550 \leq 1024 = 2^{10} \Rightarrow 10 \text{ bits}$$

b) What are the minimum number of bits required to represent source register (SR) and destination register (DR)?

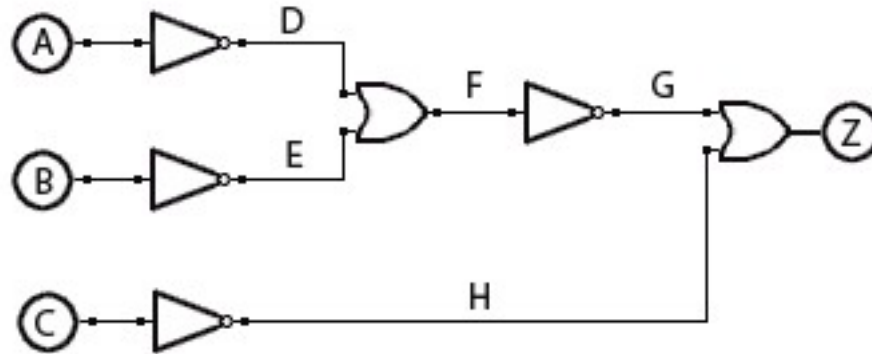
$$32 = 2^5 \Rightarrow 5 \text{ bits}$$

c) (2 points) What is the range of values that can be represented by the immediate (IMM)? Assume IMM is a two's complement value.

$$32 - (10 + 5 + 5) = 12$$
$$-2^{11} \leq \text{IMM} \leq 2^{11} - 1$$

Problem 3 (4 points)

The figure below shows a combinational logic circuit. A, B, and C are the inputs to the circuit, Z is the output, and D, E, F, G, H are internal wires.



a) What is the output Z when $A = 0$, $B = 0$, $C = 1$? Explain by identifying the values of internal wires.

$$D = 1$$

$$E = 1$$

$$F = 1$$

$$G = 0$$

$$H = 0$$

$$Z = 0$$

b) What is the output Z when $C = 0$? Explain.

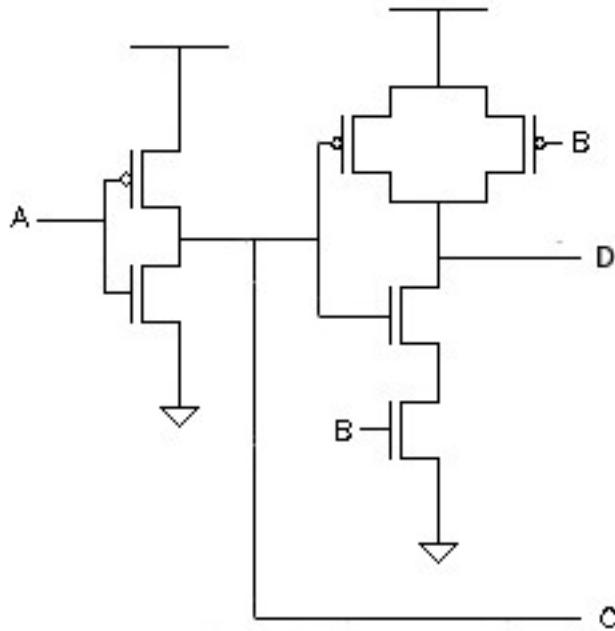
$$C = 0$$

$$H = 1$$

Z is always 1.

Problem 4 (3 points)

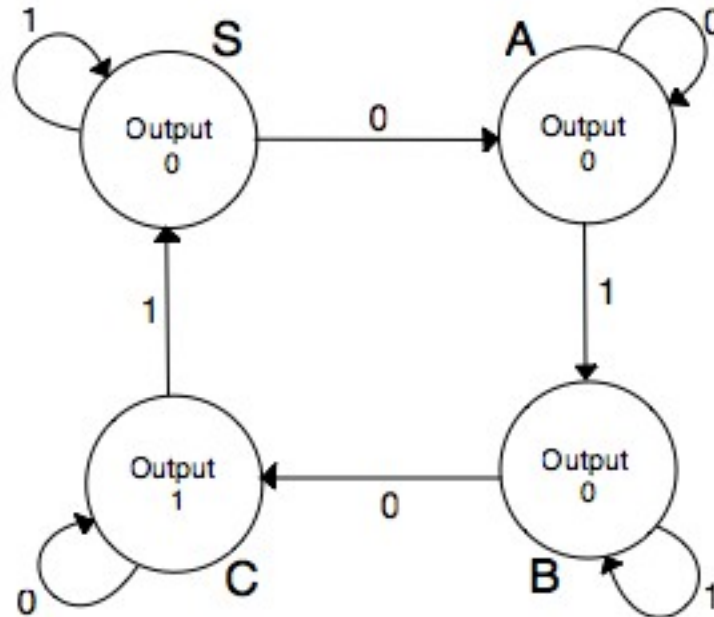
Fill in the truth table for C and D for the following transistor level circuit. Note that the two wires labeled B are assumed to be connected to each other.



A	B	C	D
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1

Problem 5 (4 points)

The figure below is a finite state machine (FSM) diagram, where the start state is S. Complete the questions according to the behavior of this machine.



a) If an input sequence is: 101000, write the state changes (eg. $S \rightarrow _ \rightarrow _ \rightarrow \dots$).

$S \rightarrow S \rightarrow A \rightarrow B \rightarrow C \rightarrow C \rightarrow C$

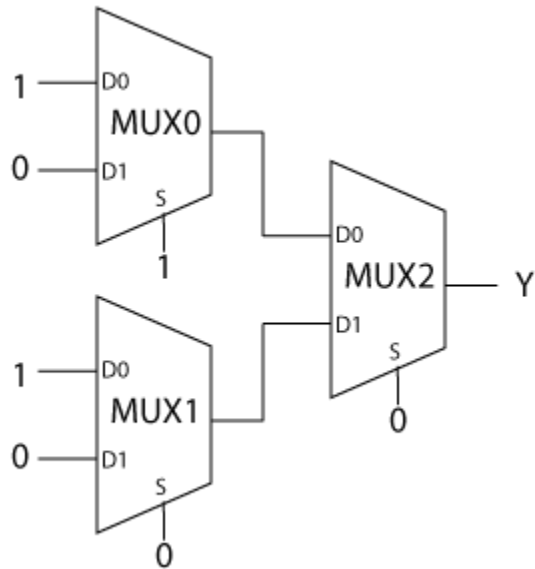
b) For the same input sequence 101000, what is the output sequence?

000111

c) (2 points) Assume the current state is A, what input sequence will put the FSM back to state S?

101

Problem 6 (3 points)



The figure above is a circuit with three 2-to-1 multiplexers. What is the output Y? Explain.

MUX0 outputs D1 value 0.

MUX1 outputs D0 value 1.

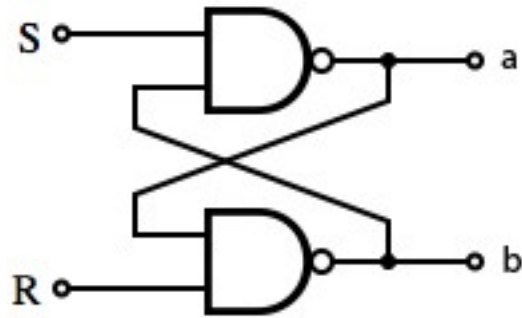
MUX2 selects D0 (MUX0's output), thus $Y = 0$.

Problem 7 (2 points)

A load to a memory uses a 7-bit address $A[6:0]$ to obtain a 14-bit value $V[13:0]$. What is the total number of bits that can be stored in all of the memory?

$$2^7 * 14 = 128 * 14 = 1792$$

Problem 8 (3 points)



a) For this R-S latch, what are the values of a and b if $S = 0$, and $R = 1$?

a = 1
b = 0

b) Then, S changes to 1 (now $S = 1$, $R = 1$). What are the values of a and b?

a = 1
b = 0

c) Then, R changes to 0 (now $S = 1$, $R = 0$). What are the values of a and b?

a = 0
b = 1

Problem 9 (4 points)

Circle the correct answer.

a) The instruction register holds the address of the instruction to be executed next. [True / **False**]

b) The LDR (load) instruction writes to a register. [**True** / False]

c) A 4-state finite state machine can be implemented using 2 D-latches. [True / **False**]

d) The ADD instruction leaves the program counter unchanged. [True / **False**]