CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING
COMPUTER SCIENCES DEPARTMENT
UNIVERSITY OF WISCONSIN-MADISON

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Midterm Examination 2
In Class (50 minutes)
Wednesday, March 14, 2007
Weight: 15%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam in two-sided and has **9** pages, including two blank pages at the end.

Plan your time carefully, since some problems are longer than others.

NAME: _____

ID# _____

Problem Number	Maximum Points	Actual Points
1	3	
2	4	
3	4	
4	3	
5	4	
6	4	
7	4	
8	4	
Total	30	

Problem 1 (3 points)

Write the Boolean expression corresponding to the following truth table. You need not simplify the expression.

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Problem 2 (4 points)

Suppose a 32-bit instruction takes the following format:

OPCODE	SR	DR	IMM

If there are 75 opcodes and 32 registers:

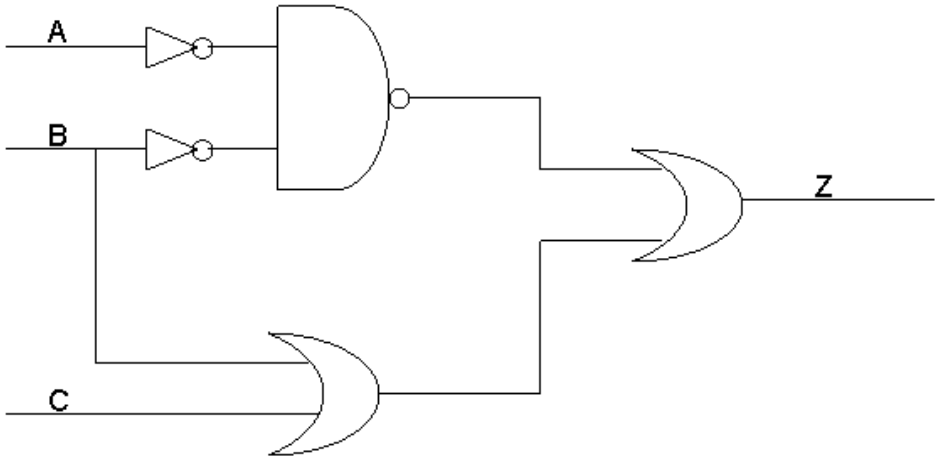
a) What is the minimum number of bits required to represent the OPCODE?

b) What are the minimum number of bits required to represent SR and DR?

c) (2 points) What is the range of values that can be represented by the immediate (IMM)? Assume IMM is a two's complement value.

Problem 3 (4 points)

The figure below shows a combinational logic circuit. Complete the truth table corresponding to this circuit. What 3-input gate is equivalent to this logic circuit?



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

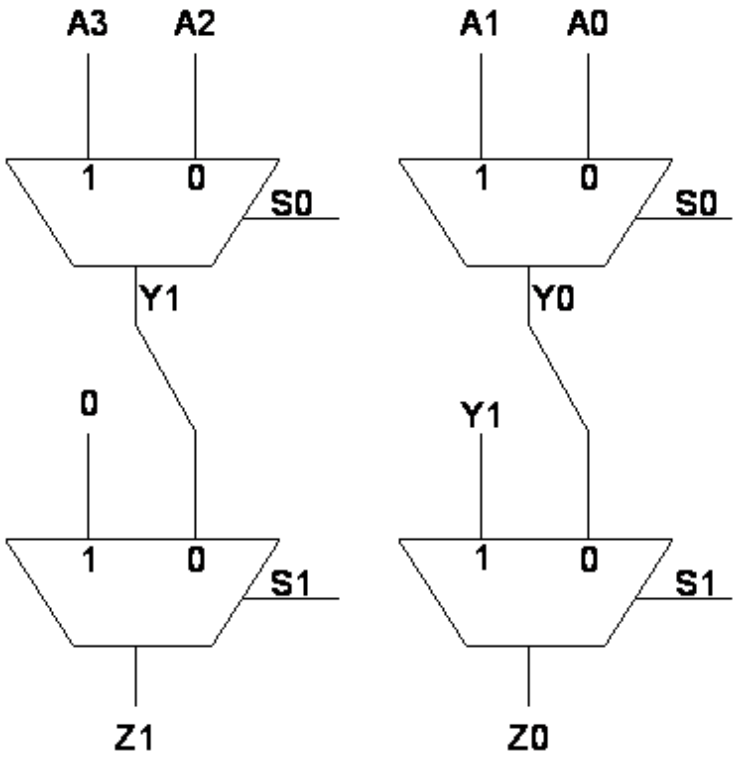
Equivalent 3-input gate is:

Problem 4 (3 points)

A load to a memory uses a 14-bit address A[13:0] to obtain a 12-bit value V[11:0]. What is the total number of bits that can be stored in all of the memory?

Problem 5 (4 points)

The figure below shows a combinational logic circuit with four 2-to-1 multiplexers. If S0 = 1 and S1 = 0, what will be the values of Z0 and Z1? Express your answer in terms of A0, A1, A2 and A3. Note that two wires with the same name are assumed to be connected to each other.

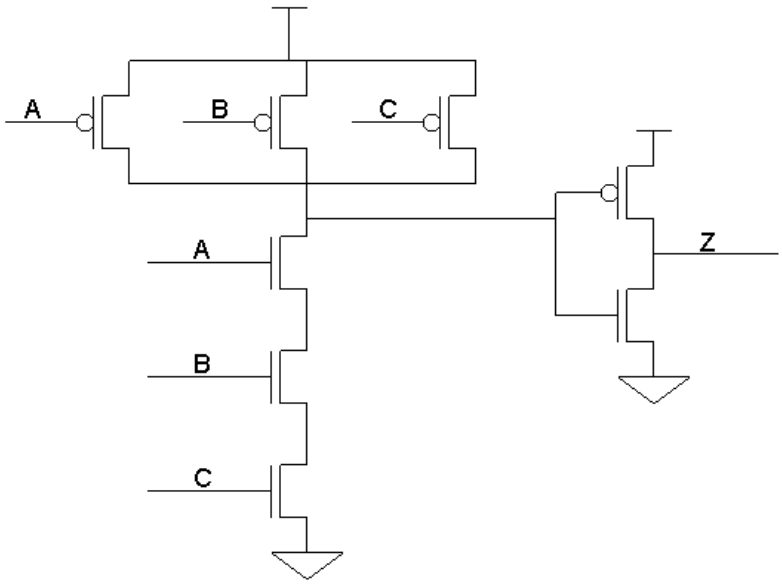


Z0 =

Z1 =

Problem 6 (4 points)

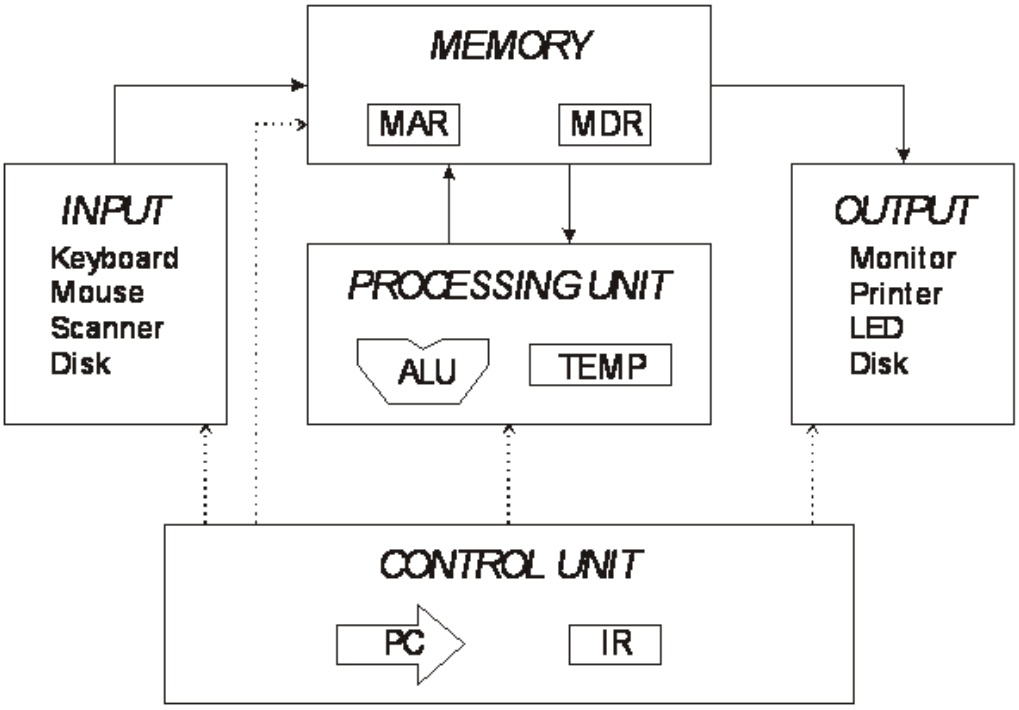
Fill in the truth table for the following transistor level circuit. Note that two wires with the same name are assumed to be connected to each other.



A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Problem 7 (4 points)

The figure below shows a block diagram of the Von Neumann model.



List the steps in the FETCH stage of instruction processing in the von Neumann model. The **bold** text below begins your answer:

Transfer contents of PC to MAR

Problem 8 (4 points)

A pattern detector is a finite state machine that outputs "1" when a particular sequence is detected and outputs "0" otherwise.

a) Draw the finite state machine diagram for a pattern detector which detects the sequence ‘10’. The pattern detector takes a single bit (1 or 0) as input every clock cycle and outputs a 1 or 0 depending on whether or not the ’10’ sequence is seen in the input stream. Thus for an input stream ‘11000101’ the output will be ‘00100010’

b) How many flip-flops (storage elements) will be needed to implement this pattern detector? Why?

Scratch Sheet 1 (in case you need additional space for some of your answers)

Scratch Sheet 2 (in case you need additional space for some of your answers)