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CS/ECE 752: Advanced Computer Architecture I

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HOMEWORK I

Due Friday 9 September 1994

Pertains to prerequite material. You should work alone. **No late assignments will be accepted.**

Problem I.1

(4 points) Implement a memory that stores 64K words of 16 bits each. Let the memory's inputs be a 16-bit `address`, `store` and `load`, while data uses a bidirectional 16-bit `data` bus. A store is performed by placing the address and data on `address` and `data` and asserting `store`; while load places the address on `address`, asserts `load`, and expects the loaded data to appear on `data`.

Use gates and a hypothetical 16Kx8bit SRAM with inputs `addr`, `read`, `write`, `chip_select` and an bidirectional 8-bit `chipdata`. Assume the chip is performs reads and writes only if `chip_select` is asserted. State any additional assumption you have to make.

Problem I.2

(6 points) Register forwarding can avoid pipeline bubbles on some data dependences in the attached standard pipeline for a conventional RISC (e.g., MIPS or DLX). Add register forwarding logic to bypass from ALU instructions (e.g., ADD) to the **lower ALU input** of ALU instructions. State any other assumptions you need to make. For more information on standard pipelines, see a computer organization text such as Hennessy & Patterson, Computer Organization and Design: The Hardware and Software Interface, Chapter 6. Turn over for pipeline diagram.

(a) *(2 points)* Add the datapath support that you need (e.g., muxes and 32-bit buses). (Load/store support has removed from the diagram to give you more room to work.)

(b) *(4 points)* Give a block diagram or gate implementation of the logic necessary to appropriately activate the bypass paths. Your logic need not work of non-ALU instructions. Assume that an instruction in IRi has register specifiers are called `IRi.ReadRegister1`, `IRi.ReadRegister2`, and `IRi.WriteRegister`. Thus, the lower ALU operand was an immediate or was read from register `IR1.ReadRegister2`.

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