

## Parallel Programming (Chapters 2, 3, & 4)

Copyright 2003 Mark D. Hill University of Wisconsin-Madison

Slides are derived from work by Sarita Adve (Illinois), Babak Falsafi (CMU), Alvy Lebeck (Duke), Steve Reinhardt (Michigan), and J. P. Singh (Princeton). Thanks!

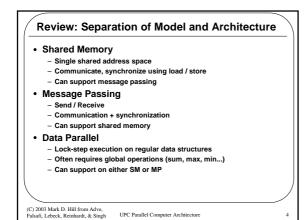
## Parallel Programming

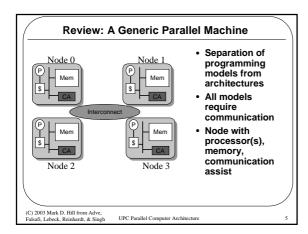
To understand and evaluate design decisions in a parallel machine, we must get <u>an idea</u> of the software that runs on a parallel machine.

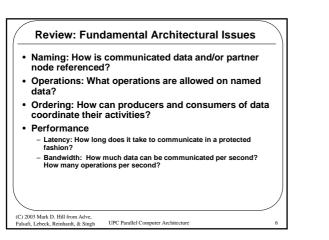
--Introduction to Culler et al.'s Chapter 2, beginning 192 pages on software

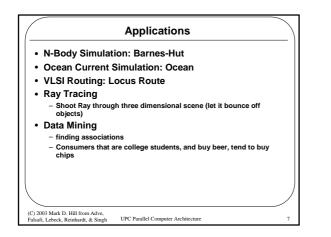
(C) 2003 Mark D. Hill from Adve, Falsafi, Lebeck, Reinhardt, & Singh UPC Parallel Computer Architecture

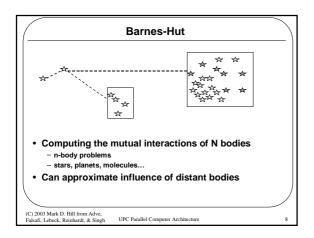
Outline	
Review	
Applications	
Creating Parallel Programs	
Programming for Performance	
• Scaling	
(C) 2003 Mark D. Hill from Adve, Falsafi, Lebeck, Reinhardt, & Singh UPC Parallel Computer Architecture	3

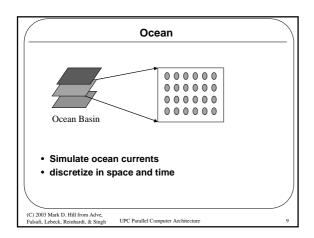




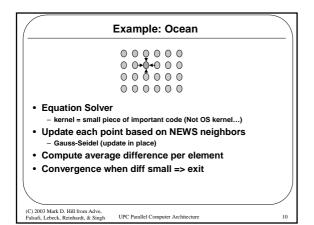


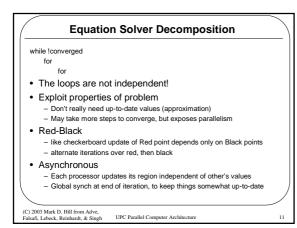


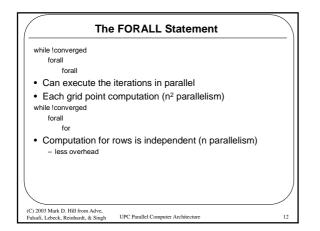


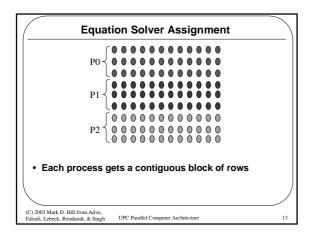




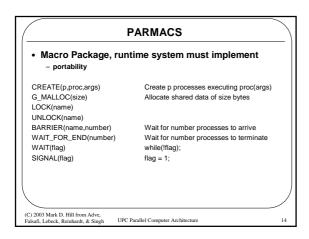


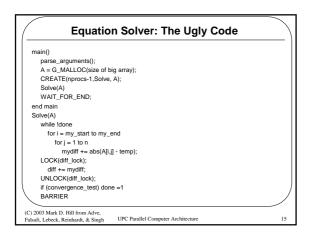


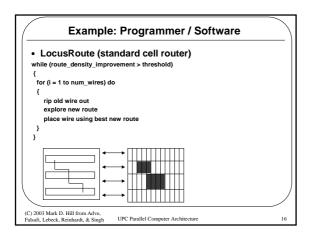




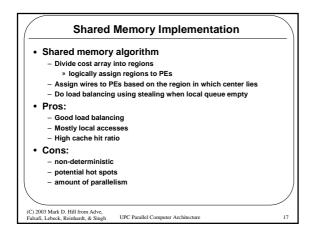


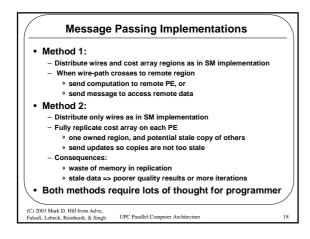


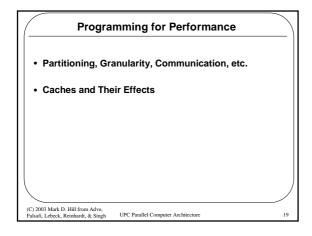


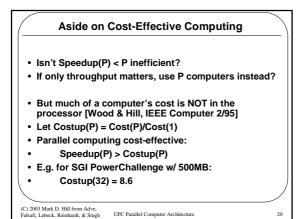


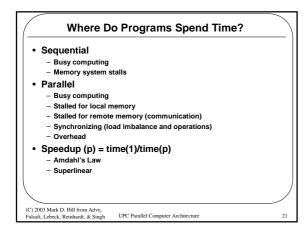


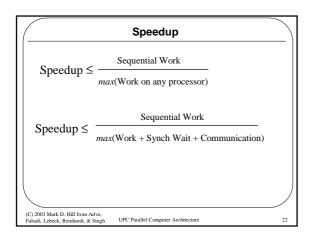


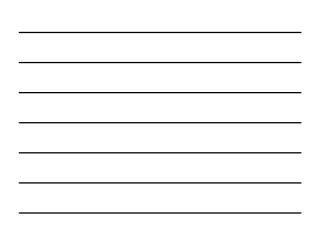


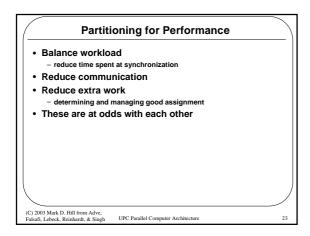


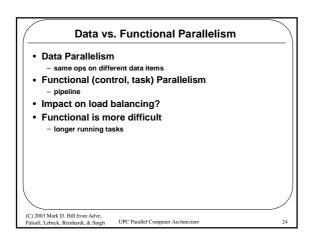




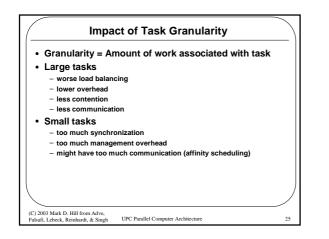


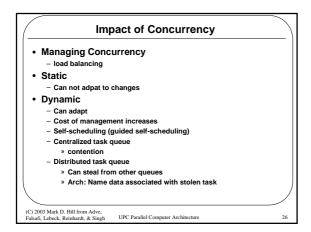


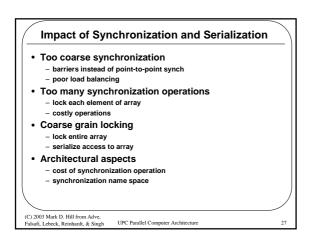


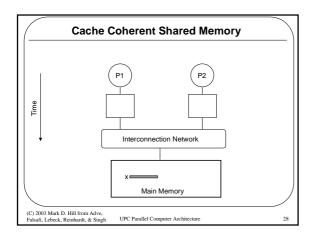




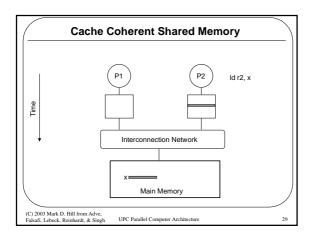




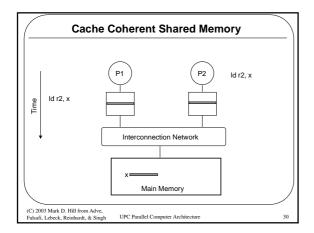




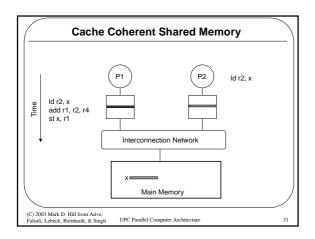




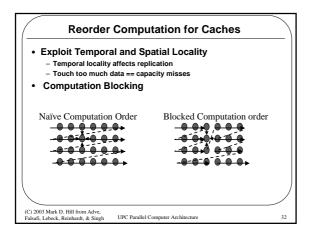




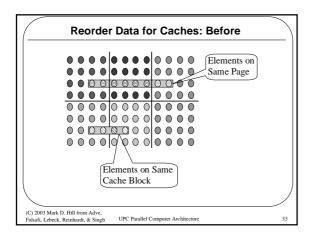


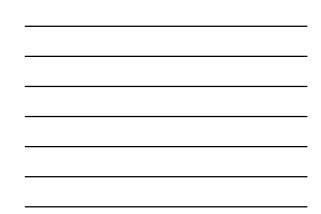


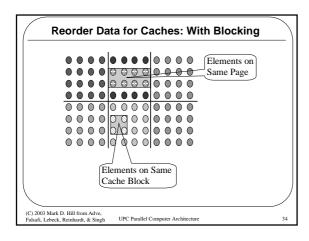




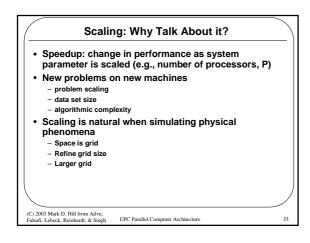


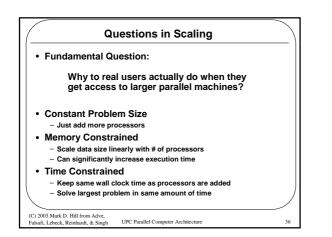


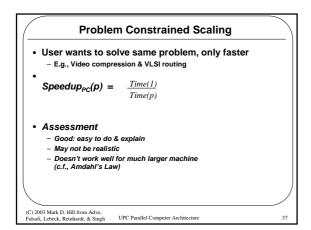


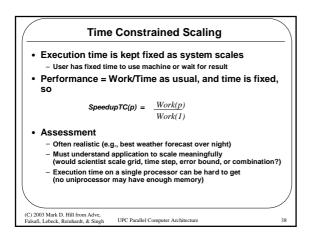


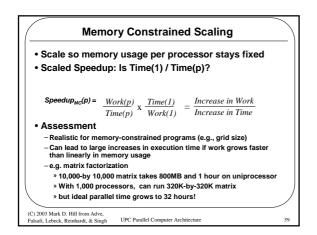


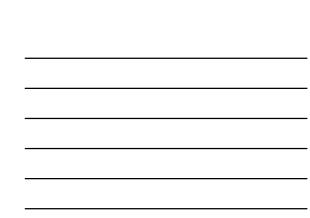












## **Scaling Down**

- · Scale down to shorten evaluation time on hardware and especially on simulators
- "Scale up" issues apply in reserve

(C) 2003 Mark D. Hill from Adve, Falsafi, Lebeck, Reinhardt, & Singh

- · Must watch out if problem size gets too small Communication dominates computation (e.g., all boundary elements)
   Problem size gets too small for realistic caches, yielding too many cache hits
  - » Scale caches down considering application working sets

UPC Parallel Computer Architecture

- » E.g., if a on a realistic problem a realistic cache could hold a matrix row but not whole matrix
  » Scale cache so it hold only row or scaled problem's matrix

The SPLASH2 Benchmarks Kernels - Complex 1D FFT - Blocked LU Factorization - Blocked Sparse Cholesky Factorization - Integer Radix Sort • Applications - Barnes-Hut: interaction of bodies - Adaptive Fast Multipole (FMM): interaction of bodies - Ocean Simulation - Hierarchical Radiosity - Ray Tracer (Raytrace) - Volume Renderer (Volrend) - Water Simulation with Spatial Data Structrue (Water-Spatial) - Water Simulation without Spatial Data Structure (Water-Nsquared) (C) 2003 Mark D. Hill from Adve, Falsafi, Lebeck, Reinhardt, & Singh UPC Parallel Computer Architecture 41