Peter Y. Hsu

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Education

Ph.D. 1985, **M.S.** 1983 in Computer Science, University of Illinois at Urbana-Champaign.
B.S. 1979 in Computer Science, University of Minnesota at Minneapolis.

Professional Experience

Consultant, *Peter Hsu Consulting, Inc.*, 2001-Present
Consultations on embedded computer organization, server system architecture, VLIW code generation techniques, and embedded DRAM technology applications.

Visiting Industrial Researcher, *University of Wisconsin at Madison,* Spring 2001
Researched advanced computer architectures. Lectured on computer design challenges.

Chief Architect, *Toshiba America Electronics Components, Inc.,* 1999-2001
Developed process-independent, fully synthesized standard-cell implementation of superscalar MIPS processor for system-on-a-chip applications.

Cofounder and **Vice President of Technology**, *ArtX Inc.,* 1997-1999
ArtX is best known for developing the 3-D graphics for the Nintendo GameCube video game platform. Also developed unified memory graphics and system controller chip for gaming PC. ArtX was acquired by ATI Technologies in 2001.

Director of Engineering, *Silicon Graphics Inc.,* 1995-1997
Manager of Architecture and Logic Design, *Silicon Graphics Inc.,* 1990-1995
Chief architect and design manager of MIPS R8000 microprocessor in the Power Challenge products. This quad-issue CMOS superscalar processor had a sophisticated data streaming architecture that revolutionized price-performance in the scientific computing market.

Member of Technical Staff, *Sun Microsystems Inc.,* 1988-1990
Advanced development of Gallium Arsenide SPARC processor with extremely low latencies for superior enterprise computing performance. Novel technology required invention of a host of new techniques and methodologies in circuit design, chip packaging, and CAD tools.

Member of Technical Staff, *Cydrome Inc.,* 1987-1988
Cydrome developed a VLIW machines in the mid 80's. Assisted in architecture definition of binary compatible second generation machine.

Member of Technical Staff, *IBM Research, Yorktown Heights,* 1985-1987
Researched branch prediction and other instruction issue rate enhancement techniques for high instruction level parallelism machines. Developed compiler code generation techniques for a superscalar RISC processor.

Research Assistant, *Coordinated Science Laboratory, University of Illinois,* 1979-1985
Thesis research one of the earliest on software pipelining, predicated execution, and speculative code hoisting technology to exploit high degree of instruction level parallelism.

Research Assistant, *Psychology Department, University of Minnesota,* 1977-1979
Designed and constructed precision digital audio sampling and playback equipment and real-time control software for human auditory experiments.

Publications

1. Peter Hsu, "TX79: A MIPS-Compatible Synthesizable Core with Multimedia Vector Extensions," *Proceedings of Microprocessor Forum*, 2000.
2. Peter Y.-T. Hsu,"Designing the TFP Microprocessor," *IEEE Micro,* Vol. 14, No. 2, 1994.
3. Peter Y.-T. Hsu, "Silicon Graphics TFP Micro-Supercomputer Chipset," *Proceedings of the Hot Chips V Conference,* 1994.
4. Ikumi, et. al., "A 300 MIPS, 300 MFLOPS Four-Issue CMOS Superscalar Microprocessor," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 1994.
5. P. Y.-T. Hsu, B. R. Rau and K. J. M. Moriarty, "Applications Development on the Very Long Instruction Word Cydra-5," *International Journal of Supercomputer Applications,* Vol. 3, No. 3, 1989.
6. James C. Dehnert, Peter Y.-T. Hsu and Joseph P. Bratt, "Overlapped Loop Support in the Cydra 5," *Third International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-III)*, Boston, Massachusetts, 1998.
7. Peter Y.-T. Hsu and Edward S. Davidson, "Highly Concurrent Scalar Processing," *Proceedings of the 13th Annual International Symposium on Computer Architecture (ISCA-13)*, Tokyo, Japan, 1986.
8. Peter Y.-T. Hsu, Joseph T. Rahmeh, Edward S. Davidson and Jacob A. Abraham, "TIDBITS: Speedup Via Time-Delayed Bit-Slicing in ALU Design for VLSI Technology," *Proceedings of the 12th Annual International Symposium on Computer Architecture (ISCA-12)*, Boston, Massachusetts, 1985.

Selected Presentations

1. "DRAM+CPU: Build It, They Will Come," keynote presentation, IEEE Computer Element Vail Workshop, Vail, Colorado, 26 June 2005.
2. "The Processor that Don't Cost a Thing," North Carolina State University, Raleigh, North Carolina, 2005.
3. "Computer Architecture From Many Perspectives," Department d'Arquitectura de Computadours, Universitat Politecnica de Catalunya (UPC), Barcelona, Spain, 2001
4. "Reviving Accumulator Architecture for High ILP Implementation," Computer Architecture Colloquium, University of Wisconsin at Madison, 2001
5. "Understanding Costs of Chip Design and Manufacture," Computer Architecture Colloquium, University of Wisconsin at Madison, 2001.
7. "A Physical Perspective of Computer Architecture," Computer Architecture Colloquium, University of Wisconsin, Madison, 2001
6. "Standard Cell Architecture for High Frequency Operation," Toshiba America Electronics Components, Inc., San Jose, California, 2001