



```
(not interrupted)
   =) Ordering : one thing happens
                         before the other
   sequence of instructions:
                                       (mov
  inst , -> load addr, reg
                                         in
                                        ×86)
   12 -> add 1, re)
   i3 _ store reg, addr
   Example run: 2 CPUs
critical: up date to shared data
section? (PU,
                                        mem
                                       balance:
     =) load => re) => load => reg
(100)

odd 1 (101)

add 2 (101)
                                         101
          ole =) 101 store =) 101
                         Problem: date
           2
                              Coutcome is not
                                  determinista
     can even pappen on
```

CPU. PC 10 ad + reg(100) Switch' add => 101 interrept Store Store => 101 of rode = Datomially Desire: lock (how to build?) =) lock ensures that only

1 thread is running

4 7 4	TIME
First Try: Spin L	oc k
int mutex = 0;	0 -> free 1 -> held
Spin Lock () { Twhile (mute) !mutex = 1;	x = = 1) test muter branch
T, test 10	Tz test 10 muler 7
muter-77	MUCK 7
both enter	f