Review:

- ~~Q4, Problem 2~~
- ~~Segmentation: what is eq?~~
- ~~Spring Mid, page 13~~
- ~~Translation (Anjing)~~
- ~~No concurrency~~
- ~~Misses, Hits TLB~~
- ~~HW exe Spring '16, #4~~

2012, Q11

- ~~Spring 16, #12~~
- ~~Spring 15, #20~~

~~2013, Q10~~

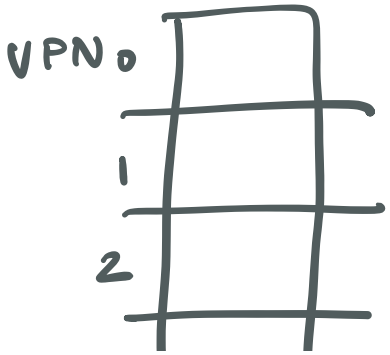
~~Fall 16, Part 7~~

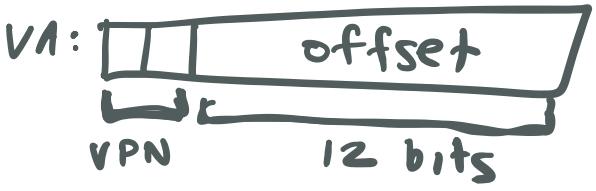
~~2018, Part 7~~

Virt. Addr. Space: 16 KB

Page Size: 4 KB

virtual address: 14 bits





2^{10} = 1024 (1 KB)

Page Table

0x8.... (valid entry)

8 bit
1000

Phys Mem: 64KB

Page Table

VPN 0 0x0...0
1 0x0....0
2 0x80...0 B
3 0x80...06

PFN

Phys Address:

16 bits
4
PA
offset
PFN (4 bits)
12 bits (4KB page)

old: 64KB phys mem
new: 256KB " "

18 bit phys addr.
6 bit PFN

VA: 0x3333

11 0011 0011 0011

VPN
12 bits
offset (use directly)

translate

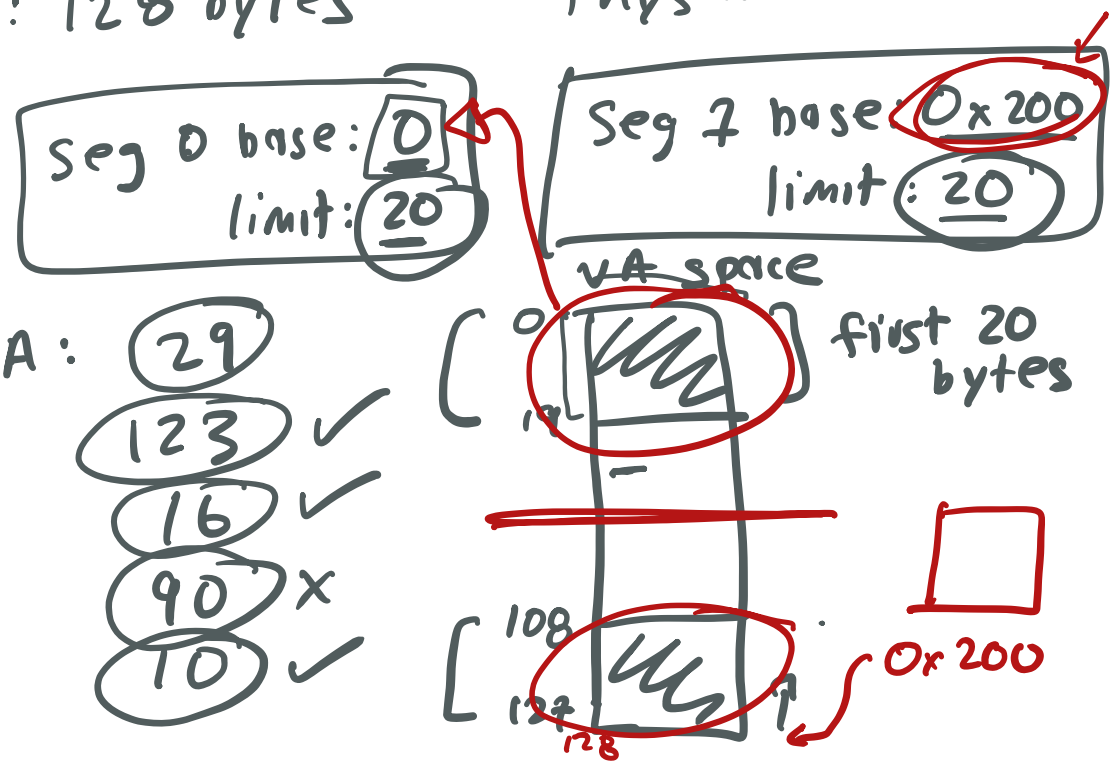
0 1 1 0

PFN

0x6333

VA: 128 bytes

Phys Mem: 512 b



0x7f 01111111 => not valid

valid

data

```
int a[4096];
int b[4096];
int c; int i;
```

code

```
for (i=0; i<4096; i++)
  c = a[i] + b[i];
```

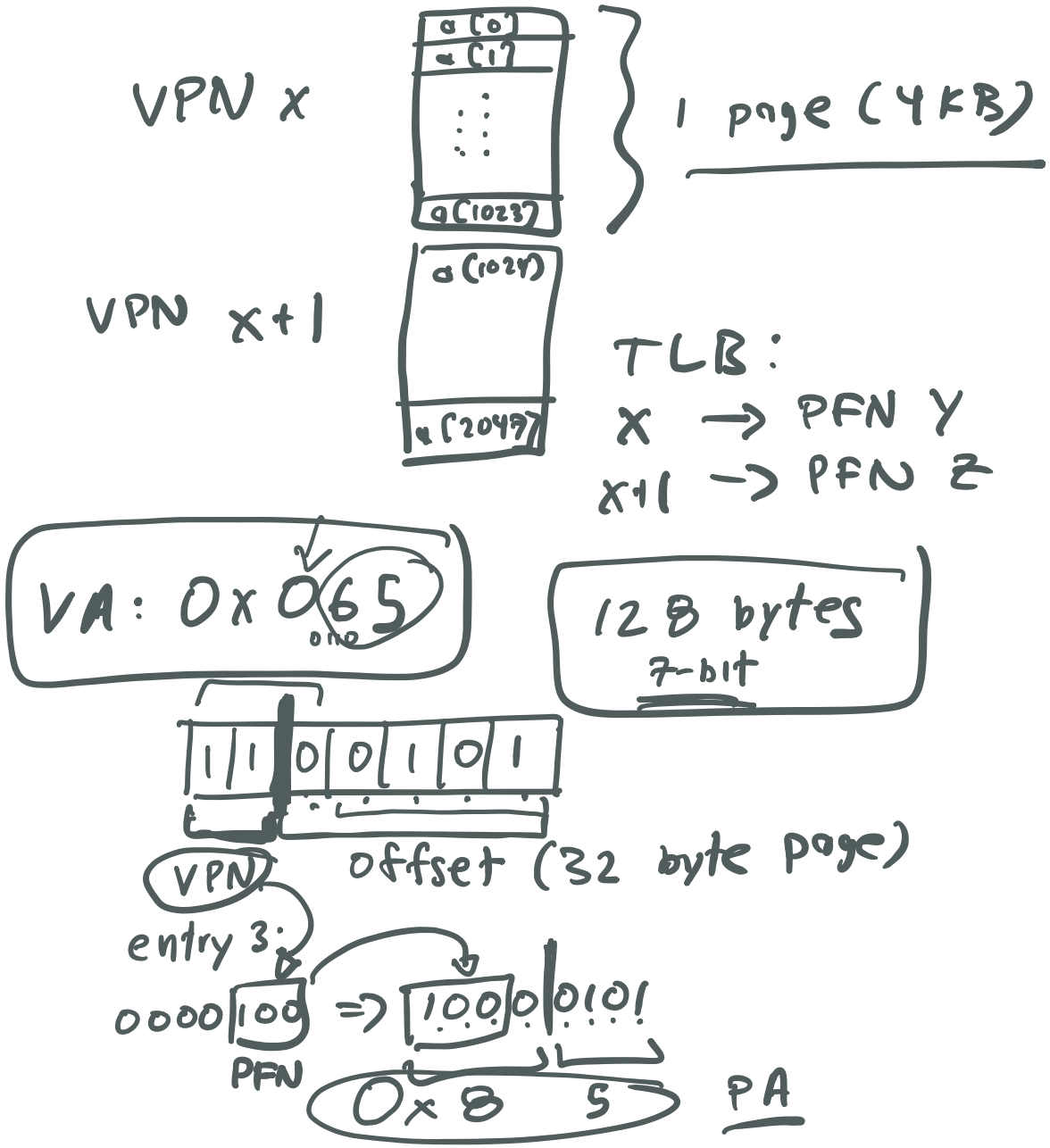
=> 1 or 2 pages

data

4 byte integers

Array: 16 KB] 4 pages

B: 16 KB] 4 pages


VPN x
a[0]
a[1]
a[1023]
1 page (4KB)
VPN x+1
a[1024]
a[2047]
TLB:
X -> PFN Y
X+1 -> PFN Z
VA: 0x065
offset
128 bytes
7-bit
1 1 0 0 1 0 1
VPN
offset (32 byte page)
entry 3:
0000 100
PFN
=> 1000 0101
0x8 5
PA