MEMORY: TLBS, SMALLER PAGETABLES

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CS 537, Spring 2019
ADMINISTRIVIA

- Project 2a is due Friday
- Project 1b grades this week
- Midterm makeup emails
AGENDA / LEARNING OUTCOMES

Memory virtualization
   What are the challenges with paging?
   How we go about addressing them?
RECAP
**Review: Match Description**

**Description**

1. one process uses RAM at a time
2. rewrite code and addresses before running
3. add per-process starting location to virt addr to obtain phys addr
4. dynamic approach that verifies address is in valid range
5. several base+bound pairs per process

**Name of approach**

- Time sharing
- Static relocation
- Base
- Base + Bounds
- Segmentation

**Candidates:** Segmentation, Static Relocation, Base, Base+Bounds, Time Sharing
FRAGMENTATION

Definition: Free memory that can’t be usefully allocated

Types of fragmentation
External: Visible to allocator (e.g., OS)
Internal: Visible to requester

Not Compacted

<table>
<thead>
<tr>
<th>Size</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0KB</td>
<td>Operating System</td>
</tr>
<tr>
<td>8KB</td>
<td>(not in use)</td>
</tr>
<tr>
<td>16KB</td>
<td>(not in use)</td>
</tr>
<tr>
<td>24KB</td>
<td>Allocated</td>
</tr>
<tr>
<td>32KB</td>
<td>(not in use)</td>
</tr>
<tr>
<td>40KB</td>
<td>Allocated</td>
</tr>
<tr>
<td>48KB</td>
<td>(not in use)</td>
</tr>
<tr>
<td>56KB</td>
<td>Allocated</td>
</tr>
<tr>
<td>64KB</td>
<td>Allocated</td>
</tr>
</tbody>
</table>
Goal: Eliminate requirement that address space is contiguous
   Eliminate external fragmentation
   Grow segments as needed

Idea:
Divide address spaces and physical memory into fixed-sized pages

Size: $2^n$, Example: 4KB
What is a good data structure?

Simple solution: Linear page table aka array

Page table per process

Address format

Page Table Entry

VPN

$2^n$
PAGING TRANSLATION STEPS

For each mem reference:

1. extract **VPN** (virt page num) from **VA** (virt addr)
2. calculate addr of **PTE** (page table entry)
3. read **PTE** from memory
4. extract **PFN** (page frame num)
5. build **PA** (phys addr)
6. read contents of **PA** from memory into register

\[10 \rightarrow \text{offset of 2}\]
MEMORY ACCESSES WITH PAGING

Assume PT is at phys addr 0x3000
Assume PTE's are 4 bytes
Assume 4KB pages

How many bits for offset? 12

Simplified view of page table

Fetch instruction at logical addr 0x0040:
- Access page table to get ppn for vpn __
- Mem ref 1: 0x3000
- Learn vpn □ is at ppn __
- Fetch instruction at □, 2040 (Mem ref 2)

Exec, load from logical addr 0x1400
- Access page table to get ppn for vpn __
- Mem ref 3: 0x3004
- Learn vpn □ is at ppn __
- Movl from _____ into reg (Mem ref 4)
QUIZ: HOW BIG IS A PAGETABLE?

How big is a typical page table?
- assume 32-bit address space
- assume 4 KB pages
- assume 4 byte entries
DISADVANTAGES OF PAGING

Additional memory reference to page table → Very inefficient
- Page table must be stored in memory
- MMU stores only base address of page table

Storage for page tables may be substantial
- Simple page table: Requires PTE for all pages in address space
  Entry needed even if page not allocated?
Example: Array Iterator

```c
int sum = 0;
for (i=0; i<N; i++) {
    sum += a[i];
}
```

What virtual addresses?
- 0x3000
- 0x3004
- 0x3008
- 0x300C

What physical addresses?
- load 0x100C
- load 0x7000
- load 0x100C
- load 0x7004
- load 0x100C
- load 0x7008
- load 0x100C
- load 0x700C

Assume ‘a’ starts at 0x3000.
Ignore instruction fetches and access to ‘i’.
STRATEGY: CACHE PAGE TRANSLATIONS
TLB: TRANSLATION LOOKASIDE BUFFER
TLB ORGANIZATION

TLB Entry

<table>
<thead>
<tr>
<th>Tag (virtual page number)</th>
<th>Physical page number (page table entry)</th>
</tr>
</thead>
</table>

Fully associative

Any given translation can be anywhere in the TLB
Hardware will search the entire TLB in parallel

Similar in design

Physical page number

Virtual page number
int sum = 0;
for (i = 0; i < 2048; i++){
    sum += a[i];
}

Assume ‘a’ starts at 0x1000
Ignore instruction fetches and access to ‘i’

What will TLB behavior look like?
TLB ACCESSES: SEQUENTIAL EXAMPLE

CPU's TLB

<table>
<thead>
<tr>
<th>Valid</th>
<th>VPN</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

Virt

| load 0x1000 |
| load 0x1004 |
| load 0x1008 |
| load 0x100c |
| ...         |
| load 0x2000 |
| load 0x2004 |

Phys

| TLB Miss 0x0004 |
| TLB Miss 0x0008 |
| TLB Hit 0x5004 |
| TLB Miss 0x5000 |
| load 0x4000    |

Page Table

PBR 0x0000

PTBR

0 KB

4 KB

8 KB

12 KB

16 KB

20 KB

24 KB

28 KB

P1

P1

P1

P2

P2

P2

P1

P2

P1

P1

P2

P2

PT

PT

PT
TLB ACCESSES: SEQUENTIAL EXAMPLE

CPU's TLB

<table>
<thead>
<tr>
<th>Valid</th>
<th>VPN</th>
<th>PPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

PTBR

PT  P1 pagetable

0 1 5 4 ...

0 KB PT
4 KB PT
8 KB P1
12 KB P2
16 KB P2
20 KB P1
24 KB P1
28 KB P2

Virt
load 0x1000
load 0x1004 (TLB hit)
load 0x1008 (TLB hit)
load 0x100c
...
load 0x2000 (TLB hit)
load 0x2004

Phys
load 0x0004 (TLB hit)
load 0x5000
load 0x5004 (TLB hit)
load 0x5008 (TLB hit)
load 0x500C
...
load 0x0008 (TLB hit)
load 0x4000
load 0x4004
**PERFORMANCE OF TLB?**

Miss rate of TLB: \( \frac{\text{#TLB misses}}{\text{#TLB lookups}} \)

# TLB lookups? number of accesses to \( a \) = \( 2048 \)

# TLB misses?

\[ \text{= number of unique pages accessed} \]

\[ \frac{2048 \times 4}{4K} = \frac{8K}{4K} = 2 \]

Miss rate?

\[ = \frac{2}{2048} \approx \frac{2}{2000} = 0.1\% \]

Hit rate?

\[ = 1 - \text{miss rate} = 99.9\% \]

Would hit rate get better or worse with smaller pages?
TLB PERFORMANCE WITH WORKLOADS

Sequential array accesses almost always hit in TLB
  – Very fast!

What access pattern will be slow?
  – Highly random, with no repeat accesses
**Workload Access Patterns**

**Workload A**

```c
int sum = 0;
for (i=0; i<2048; i++) {
    sum += a[i];
}
```

**Workload B**

```c
int sum = 0;
srand(1234);
for (i=0; i<1000; i++) {
    sum += a[rand() % N];
}
srand(1234);
for (i=0; i<1000; i++) {
    sum += a[rand() % N];
}
```
WORKLOAD ACCESS PATTERNS

Spatial Locality
Sequential Accesses

Temporal Locality
Repeated Random Accesses
WORKLOAD LOCALITY

**Spatial Locality**: future access will be to nearby addresses

**Temporal Locality**: future access will be repeats to the same data

What TLB characteristics are best for each type?

**Spatial**:
- Access same page repeatedly; need same vpn $\rightarrow$ ppn translation
- Same TLB entry re-used

**Temporal**:  
- Access same address near in future
- Same TLB entry re-used in near future
- How near in future? How many TLB entries are there?
TLB REPLACEMENT POLICIES

**LRU**: Evict Least-Recently Used TLB slot when needed

(More on LRU later in policies next week)

**Random**: Evict randomly chosen entry

Which is better?

Simple. Is this effective?
LRU TROUBLES

Workload repeatedly accesses same offset (0x01) across 5 pages (strided access), but only 4 TLB entries

What will TLB contents be over time?
How will TLB perform?
TLB REPLACEMENT POLICIES

LRU: evict Least-Recently Used TLB slot when needed
(More on LRU later in policies next week)

Random: Evict randomly chosen entry

Sometimes random is better than a “smart” policy!
What happens if a process uses cached TLB entries from another process?

1. **Flush TLB on each switch**
   - Costly; lose all recently cached translations

2. **Track which entries are for which process**
   - Address Space Identifier
   - Tag each TLB entry with an 8-bit ASID
   - How many ASIDs do we get? Why not use PIDs?
TLB EXAMPLE WITH ASID

Virtual load 0x1444 ASID: 12

Physical 0x2444 0x5444

PTBR

<table>
<thead>
<tr>
<th>Virtual</th>
<th>Phys</th>
<th>ASID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Context switches are expensive
Even with ASID, other processes “pollute” TLB
- Discard process A’s TLB entries for process B’s entries

Architectures can have multiple TLBs
- 1 TLB for data, 1 TLB for instructions
- 1 TLB for regular pages, 1 TLB for “super pages”
HW AND OS ROLES

Who Handles TLB MISS? **H/W** or **OS**?

**H/W**

CPU must know where pagetables are
- CR3 register on x86
- Pagetable structure fixed and agreed upon between HW and OS
- HW “walks” the pagetable and fills TLB
HW AND OS ROLES

Who Handles TLB MISS?  H/W or OS?

OS:

- CPU traps into OS upon TLB miss
- “Software-managed TLB”
- OS interprets pagetables as it chooses
- Modifying TLB entries is privileged
- Need same protection bits in TLB as pagetable - rwx
Pages are great, but accessing page tables for every memory access is slow.

Cache recent page translations → TLB
- Hardware performs TLB lookup on every memory access.

TLB performance depends strongly on workload:
- Sequential workloads perform well.
- Workloads with temporal locality can perform well.

In different systems, hardware or OS handles TLB misses.

TLBs increase cost of context switches:
- Flush TLB on every context switch.
- Add ASID to every TLB entry.
DISADVANTAGES OF PAGING

Additional memory reference to page table → Very inefficient
- Page table must be stored in memory
- MMU stores only base address of page table

Storage for page tables may be substantial
- Simple page table: Requires PTE for all pages in address space
  Entry needed even if page not allocated?
SMALLER PAGE TABLES
QUIZ: HOW BIG ARE PAGE TABLES?

1. PTE’s are **2 bytes**, and **32** possible virtual page numbers

2. PTE’s are **2 bytes**, virtual addrs are **24 bits**, pages are **16 bytes**

3. PTE’s are **4 bytes**, virtual addrs are **32 bits**, and pages are **4 KB**

4. PTE’s are **4 bytes**, virtual addrs are **64 bits**, and pages are **4 KB**

How big is each page table?
WHY ARE PAGE TABLES SO LARGE?

Waste!

Virt Mem

code

heap

stack

Phys Mem
MANY INVALID PT ENTRIES

<table>
<thead>
<tr>
<th>PFN</th>
<th>valid</th>
<th>prot</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>r-x</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>rw-</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>rw-</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>rw-</td>
</tr>
</tbody>
</table>

…many more invalid…

how to avoid storing these?
Avoid Simple Linear Page Tables?

Use more complex page tables, instead of just big array

Any data structure is possible with software-managed TLB

- Hardware looks for vpn in TLB on every memory access
- If TLB does not contain vpn, TLB miss
  - Trap into OS and let OS find vpn->ppn translation
  - OS notifies TLB of vpn->ppn for future accesses
OTHER APPROACHES

1. Segmented Pagetables
2. Multi-level Pagetables
   - Page the page tables
   - Page the pagetables of page tables…
3. Inverted Pagetables
Note “hole” in addr space: valids vs. invalids are clustered

How did OS avoid allocating holes in phys memory?

Segmentation
COMBINE PAGING AND SEGMENTATION

Divide address space into segments (code, heap, stack)
   – Segments can be variable length
Divide each segment into fixed-sized pages
Logical address divided into three portions

<table>
<thead>
<tr>
<th>seg # (4 bits)</th>
<th>page number (8 bits)</th>
<th>page offset (12 bits)</th>
</tr>
</thead>
</table>

Implementation
• Each segment has a page table
• Each segment track base (physical address) and bounds of the page table
## Quiz: Paging and Segmentation

<table>
<thead>
<tr>
<th>seg # (4 bits)</th>
<th>page number (8 bits)</th>
<th>page offset (12 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>seg</td>
<td>base</td>
<td>bounds</td>
</tr>
<tr>
<td>0</td>
<td>0x002000</td>
<td>0xff</td>
</tr>
<tr>
<td>1</td>
<td>0x000000</td>
<td>0x00</td>
</tr>
<tr>
<td>2</td>
<td>0x001000</td>
<td>0x0f</td>
</tr>
</tbody>
</table>

- 0x002070 read:
- 0x202016 read:
- 0x104c84 read:
- 0x010424 write:
- 0x210014 write:
- 0x203568 read:
ADVANTAGES OF PAGING AND SEGMENTATION

Advantages of Segments
– Supports sparse address spaces.
– Decreases size of page tables. If segment not used, not need for page table

Advantages of Pages
– No external fragmentation
– Segments can grow without any reshuffling
– Can run process when some pages are swapped to disk (next lecture)

Advantages of Both
– Increases flexibility of sharing
  • Share either single page or entire segment
  • How?
DISADVANTAGES OF PAGING AND SEGMENTATION

Potentially large page tables (for each segment)
- Must allocate each page table contiguously
- More problematic with more address bits
- Page table size?
  • Assume 2 bits for segment, 18 bits for page number, 12 bits for offset

Each page table is:
= Number of entries * size of each entry
= Number of pages * 4 bytes
= 2^18 * 4 bytes = 2^20 bytes = 1 MB!!!
OTHER APPROACHES

1. Segmented Pagetables
2. Multi-level Pagetables
   - Page the page tables
   - Page the pagetables of page tables…
3. Inverted Pagetables
MULTILEVEL PAGE TABLES

Goal: Allow each page tables to be allocated non-contiguously

Idea: Page the page tables
  – Creates multiple levels of page tables; outer level “page directory”
  – Only allocate page tables for pages in use
  – Used in x86 architectures (hardware can walk known structure)
Multilevel Page Tables

30-bit address:

- outer page (8 bits)
- inner page (10 bits)
- page offset (12 bits)

base of page directory
### QUIZ: MULTILEVEL

<table>
<thead>
<tr>
<th>page directory</th>
<th>page of PT (@PPN:0x3)</th>
<th>page of PT (@PPN:0x92)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPN</td>
<td>valid</td>
<td>PPN</td>
</tr>
<tr>
<td>0x3</td>
<td>1</td>
<td>0x10</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0x23</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0x80</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0x59</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-</td>
</tr>
</tbody>
</table>

20-bit address:

| outer page(4 bits) | inner page(4 bits) | page offset (12 bits) |
QUIZ: ADDRESS FORMAT FOR MULTILEVEL PAGING

30-bit address:

<table>
<thead>
<tr>
<th>outer page</th>
<th>inner page</th>
<th>page offset (12 bits)</th>
</tr>
</thead>
</table>

How should logical address be structured?

– How many bits for each paging level?

Goal?

– Each page table fits within a page
– PTE size * number PTE = page size
  • Assume PTE size = 4 bytes
  • Page size = $2^{12}$ bytes = 4KB
  • $2^2$ bytes * number PTE = $2^{12}$ bytes
  • $\rightarrow$ number PTE = $2^{10}$
– $\rightarrow$ # bits for selecting inner page = 10

Remaining bits for outer page:

– $30 - 10 - 12 = 8$ bits
Problem with 2 levels?

Problem: page directories (outer level) may not fit in a page

64-bit address:

| outer page? | inner page (10 bits) | page offset (12 bits) |

Solution:

- Split page directories into pieces
- Use another page dir to refer to the page dir pieces.

VPN

| PD idx 0 | PD idx 1 | PT idx | OFFSET |

How large is virtual address space with 4 KB pages, 4 byte PTEs, each page table fits in page given 1, 2, 3 levels?

4KB / 4 bytes → 1K entries per level

1 level: 1K * 4K = 2\(^{22}\) = 4 MB

2 levels: 1K * 1K * 4K = 2\(^{32}\) ≈ 4 GB

3 levels: 1K * 1K * 1K * 4K = 2\(^{42}\) ≈ 4 TB
On TLB miss: lookups with more levels more expensive
Assume 3-level page table
Assume 256-byte pages
Assume 16-bit addresses
Assume ASID of current process is 211

How many physical accesses for each instruction? (Ignore previous ops changing TLB)

(a) 0xAA10: movl 0x1111, %edi

(b) 0xBB13: addl $0x3, %edi

(c) 0x0519: movl %edi, 0xFF10
INVERTED PAGE TABLE

Only need entries for virtual pages w/ valid physical mappings

Naïve approach:
Search through data structure <ppn, vpn+asid> to find match
Too much time to search entire table

Better:
Find possible matches entries by hashing vpn+asid
Smaller number of entries to search for exact match

Managing inverted page table requires software-controlled TLB
OTHER APPROACHES

1. Segmented Pagetables
2. Multi-level Pagetables
   – Page the page tables
   – Page the pagetables of page tables…
3. Inverted Pagetables
NEXT STEPS

Project 2a: Due Friday

Next class: Better pagetables, swapping!