Errata for "Architecture Design for Soft Errors," by Shubu Mukherjee, Dated May 7th, 2009

Chapter 1, Page 12, h(t) equation should read as (the negative sign before the last term is missing):

$$h(t) = P(t < T \leq t + \Delta t \mid (T > t)) = \frac{\frac{dE(t)}{dt}}{N_t} = \frac{\frac{\frac{dE(t)}{dt}}{N_0}}{\frac{N_t}{N_0}} = -\frac{\frac{dR(t)}{dt}}{R(t)}$$

Chapter 1, Page 12, last sentence, 2nd last paragraph should read as: "The expectation of R(t) is the MTTF and is equal to $1/\lambda$"

Chapter 1, Page 13, EXAMPLE and SOLUTION should read as:

EXAMPLE If the MTTR of a system is 30 seconds, how many crashes can it sustain per year and still maintain a five 9s uptime? What is the MTTF in this case?

SOLUTION A five 9s uptime denotes a total downtime of about 5 minutes per year. Hence, the number of crashes allowed for this system per year is (5 x 60 / 30) = 10. The MTTF is (1 year - 5 minutes) ~= 8759.92 hours.

Chapter 1, Page 25, last sentence of caption of Figure 1.10 should read as: "The area under the curve gives a total neutron flux of about 14 neutrons/cm^2-hour.

Chapter 1, Page 37, Section 1.10.2 DRAM Scaling Trends, first paragraph, second sentence should read as: "DRAM cells are typically made of one transistor and one storage capacitor (as opposed to six-transistor SRAMs)."

Chapter 2, Page 54, in the equation for I(t), p should be replaced with: "Square Root(π)"

Chapter 2, Page 63, Figure 2.13 caption last sentence should read as: "Copyright © 2004 IEEE"

Chapter 2, Page 64, Figure 2.14 caption last sentence should read as: "Copyright © 2004 IEEE"

Chapter 3, Page 83, 1st sentence of Section 3.4.1 should read as: "Mathematically, one can express the SDC FIT rate of a storage cell as follows:"

Chapter 3, Page 86, 2nd sentence of EXAMPLE should read as: "The SDC and DUE FIT for the chip before adding parity are 3100 and 0 FIT, respectively."

Chapter 3, Page 100, 2nd last sentence of 2nd last paragraph should read as: " ... in the commit table is 0.012 x 30 = 0.36."

Chapter 4, Page 127, Figure 4.4, un-ACE entry in table for Store Buffer should read as: "idle, evict-to-fill"

Chapter 4, Page 129, 3rd sentence of 2nd paragraph should read as: "Read-to-evict time may be ACE, unlike in a write-through cache."

Chapter 4, Page 149, last paragraph, 3rd last sentence should read as: " ..., then on average, Y% of the experiments would return a result within X% of the true value of the random variable."

Chapter 5, Page 163, 2nd last paragraph, last sentence should read as: "Then, let us define the code bits as:

code bit 1 = data bit
code bit 2 = NOT (data bit)"

Chapter 5, Page 165, 3rd last sentence of 2nd bullet should read as: "... Hamming distance of 2 away from the other valid code word of 110."

Chapter 5, Page 168, Section 5.2.2, the equation should read as: Even parity code = $a_0 \oplus a_1 \oplus \ldots \oplus a_{k-1}$

Chapter 5, Page 172, the error positions in the vector E^T should have been denoted in bold. The error position in the first equation for S should be in the E^T column in the 4th position (which is a zero) from the top. The error position in the second equation for S should be in the E^T column in the 3rd position (which is also a zero) from the top.

Chapter 5, Page 179, 1st sentence of 3rd paragraph should read as: "The CRC encoding process involves dividing $D(x).x^r$ by G(x) ..."

Please email corrections and bug fixes to shubu.mukherjee@intel.com. Many thanks to Prof. William Robinson from Vanderbilt University for his help in fixing many of these bugs.