University of Wisconsin-Madison

CS/ECE 552: Introduction to Computer Architecture

Spring 1992

End-Term Examination

May 7, 1992

Name (**Please PRINT**):_____

Limit your answers to the space provided. If you use more space than is provided, you are probably doing something wrong. Use the back of each page for any scratch work.

Problem Number	Maximum Points	Your Score
Q1	20	
Q2	22	
Q3	16	
Q4	12	
Q5	20	
Q6	10	
Total	100	

[1] (**20 points**)
Short Questions. Identify the following concepts. Most answers are one or two *words*. Your answers should be limited to 5 *words*. You will be *credited* 2 points for each *correct* answer, and *penalized* 1 point for an *incorrect* answer. The minimum score for this question will be zero. **It is possible that you may perceive a question to be ambiguous. If that happens, please state any assumptions that you make in your answer**.

i) An I/O configuration where I/O devices are treated as memory locations.

ii) A method of data transfer between an I/O device and the memory in which the data transfer is carried out explicitly by the CPU.

iii) Device used to carry out data transfers between high-speed, synchronous I/O devices and the memory.

iv) Scheme used to facilitate address translation of instruction references (for which successive references typically fall on the same page as the previous reference). This scheme is generally not effective for data references.

v) Hardware setup for priority resolution in which devices "close" to the CPU have an advantage over devices "further" from the CPU for CPU attention.

vi) Scheme used to increase the bandwidth of the memory system using memory chips of a fixed response time.

vii) Truncation scheme discussed in class with a zero bias but large maximum error.

viii) A method for speeding up the multiplication of two *streams* of numbers.

ix) Multiplication method that allows for uniform treatment of positive and negative multipliers.

x) Property of memory references in a program which allows memory hierarchies to be effective.

BE PRECISE!

[2] Short Questions (**22 points**)

(i) What is an advantage of using memory mapped I/O? **(3 points)**

(ii) What is the *main* difference between a trap and an interrupt? **(3 points)**

(iii) Consider an I/O device connected through a DMA controller to the CPU-memory bus. Would you give the DMA controller or the CPU a higher priority for access to the bus? Explain. **(3 points)**

(iv) A memory system has a total of 64 chips. Each memory chip has 8 address lines and 8 data lines. How many *bits* of memory are present in the memory system? Show your work. **(5 points)**

(v) Show the modified Booth encoding for the 8-bit numbers 29 and -12. **(4 points)**

(vi) Give 2 reasons why memory chips are typically organized as x1 chips in preference to x4 or x8 organizations. **(4 points)**

BE PRECISE!

[3] (**16 points**)
A floating point word is 39 bits long (including the sign bit). It uses a sign magnitude mantissa (or fraction), and an excess exponent to represent an arbitrary floating point number X. The base of the number system is 8. The range of of non-zero numbers that is representable (the mantissae are normalized) is given by:

$$\text{range} = \frac{X_{max}}{X_{min}} \approx 2^{6144}$$

where X_{max} is the largest, positive number, and X_{min} is the smallest (non-zero) positive number.

(i) How many bits does the mantissa have, not including the sign bit? Show your work and reasoning. **(8 points)**.

(ii) Again assuming standard normalization, what is the total number of floating-point numbers that can be represented in this format? Show your work and reasoning. **(4 points)**.

(iii) Suppose that *denormalized* numbers are allowed in this format. Approximately how many positive denormalized numbers are possible? Show your work and reasoning. **(4 points)**.

BE PRECISE!

[4] (**12 points**)
The parity check matrix for a SECDED Hamming code is given below. In this matrix C_i's denote check bits and b_i's denote information bits. *Note that the location of these bits is different form those discussed in the class and hence the syndrome discussed in class may not be applicable.* The code-words are stored in memory in the same bit order as shown in the parity check matrix.

	C_1	C_2	C_3	C_4	b_1	b_2	b_3	b_4
	1	0	0	0	1	1	0	1
H=	0	1	0	0	1	0	1	1
	0	0	1	0	0	1	1	1
	1	1	1	1	1	1	1	1

(i) For the above code, what is the correct code word for the following words read from memory, assuming that at most *two* bits can be in error. If it is not possible to give the correct code word, say so and give your reason.

(a) Word read from memory = 0101 1011. **(3 points)**

(b) Word read from memory = 0110 0101. **(3 points)**

(ii) The memory of a computer system has a data word with 27 bits. What is the *minimum* number of check bits needed to implement a *single error correction (SEC)* scheme? The check bits should be able to correct single bit errors in both the data and the check bits. **(4 points)**

How many check bits are required if you need to correct errors only in the data bits? **(2 points)**

BE PRECISE!

[5] (**20 points**)

(i) A computer system has a 32K byte, 8-way set associative cache, and the block size is 8 bytes. The machine is byte addressable, and physical addresses generated by the CPU are 22 bits. Specify how the physical address is partitioned into tag, set, and offset fields, giving the number of bits in each field. **(6 points)**

(ii) Does it make sense to have a 3-way set associative cache? Why or why not? (**No credit without explanation**). **(6 points)**

(iii) Assume that you have an unlimited number of carry save adder (CSA) units (with a delay of 2d) and an unlimited number of carry lookahead adder (CLA) units (with a delay of 12d). Sketch the design of a FAST multiplier to multiply two 16-bit numbers, and calculate the delay through the multiplier. **(8 points)**

BE PRECISE!

[6] **True and False Questions** (**10 points**)
For each of the following statements, answer **TRUE(T)** if the statement is true and **FALSE(F)** if the statement is false. You will be *credited* 2 points for each *correct* answer, and *penalized* 1 point for each *incorrect* answer. **It is possible that you may perceive a question to be ambiguous. If that happens, please state any assumptions that you make in your answer**. The minimum score for this question will be zero.

(i) In a floating-point number system, a "hidden bit", i.e., a bit that is not stored in memory with a normalized mantissa, can not be used if the base of the number system is 4.

(ii) In a truncation scheme, the maximum error is more important than the bias since the maximum error accumulates with repeated truncations, whereas the bias does not.

(iii) In a floating-point number system, larger bases improve the accuracy at the cost of sacrificing the range.

(iv) In a *non-restoring* division algorithm, the number of arithmetic (add/sub) operations that is carried out is 2n, where n is the number of bits in the dividend.

(v) A page fault occurs when the virtual to physical address translation (i.e., the page table entry) can not be found in the translation lookaside buffer.