[1]

(i) memory-mapped I/O
(ii) program controlled I/O
(iii) DMA controller
(iv) pretranslation (did not cover in class)
(v) daisy chain
(vi) banking or interleaving
(vii) janmming or von Neumann rounding
(viii) array multiplier
(ix) Booth's recoding
(x) spatial and temporal locality

[2]

(i) I/O devices can be accessed with ordinary memory-accessing instructions

(ii) trap is synchronous whereas interrupt is asynchronous
(did not cover in class; covered in CS/ECE 354)

(iii) DMA controller. If CPU is given priority it could hog the bus and/or perturb a high-speed transfer that is being carried out by the DMA.
(did not cover in class)

(iv) 2**8 x 8 = 4K bits per chip. 4K x 64 = 32Kbytes total.

(v) 29 is (0 2 -1 1) and -12 is (0 -1 1 0)

(vi) (a) number of pins is minimized, (b) easier to implement error correction (e.g., a SECDED scheme) when chip is used to build bigger memory systems.

[3]

Assume that leading digit for a normalized number is to the right of the fractional point.
(This is the case with FP number systems that use bases other than 2 but is not true with IEEE FP where the leading digit is to the left of the fractional point. This does not change the calculation, however.)

(i) suppose max exponent is approximately E and min is approximately -E.

Largest number is approximately 1 x 8 ** E

Smallest is approximately 1/8 x 8 ** -E

Largest / Smallest = 8 ** (2E + 3) = 2 ** 6144

Solve for E gives E approx 1024. This means that 11 bits are used for exponent (to allow values from -1023 to 1024)

This leaves 39-11-1 = 27 bits or 9 octal digits for mantissa.

(ii) Leading digit (3 bits) has to be non-zero. 7/8 combinations of the leading digit are valid, others are not.

So total numbers is 7/8 x 2 ** 39.

(iii) Here leading digit of mantissa is 0 but other 24 bits can be anything. Moreover the exponent bits are fixed a the smallest value.

Therefore the total positive denorms are 2**24.

[4]

(i) (a) C1, C2, C3 indicate an error but C4 indicates no error so there is a double-bit error

(i) (b) Same as above. C1, C2, C3 indicate an error but C4 indicates no error so there is a double-bit error

(ii) k check bits. 2**k >= 27+k+1 so k=6. 6 check bits needed.

(iii) k check bits. 2**k >= 27+1 so k=5. 5 check bits needed.

[5]

(i) 32 KB cache / 8B blocks => 4K blocks in the cache
4K blocks / 8 ways => 512 blocks in a way => 9 bits needed for set index

8B blocks => 3 bits needed for byte addressability

bits 0 - 2 : block offset
bits 3 - 11: set index
bits 12 - 21 : tag

(ii) A set-associative cache with 3 ways is possible as long as the number of blocks in a way is a power of 2. This can be useful if budget requirements prohibit a fourth way (keeping the way size constant).

(iii) To use a Wallace Tree multiplier to multiply two 16-bit numbers, we need to add all the multipliers resulting from the multiplicand. Therefore we need to add 16 32-bit numbers. This can be done using a carry-save tree (see page 331 from the text) with 6 levels of carry-save adders and one carry lookahead adder. The total delay is 2d * 6 + 12d = 24d.

[6]

(i) T. Hidden bit can only be used for base 2

(ii) F. It is the bias that accumulates, not the max. error.

(iii) T.

(iv) F. In non-restoring division, there are only n ops. In restoring division there can be up to 2n ops.

(v) F. Page fault occurs when the page is not in main memory. If the mapping is not found in the TLB we have a TLB miss not a page fault.