University of Wisconsin-Madison

CS/ECE 552: Introduction to Computer Architecture
Spring 2005

**Syllabus for Midterm Exam**

**By Section Number**

**Chapter 1**: All sections.

**Chapter 2**: All sections.

**Chapter 3**: All sections.

**Chapter 4**: Sections 4.1, 4.2, 4.3, 4.4, 4.5.

**Chapter 5**: All sections.

**Chapter 6**: Sections 6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7.

**By Topics (Several topics are not included in the textbook)**

Concept of stored program computer, fetch-decode-execute cycle, latency and bandwidth, system balance, law of performance, principles of pipelining, register and memory address spaces.

Instruction formats and use in the MIPS architecture.

Simple computation engine, register file, data path, adders, subtractors, lookahead principles, lookahead tree structures, ALU design, barrel shifters.

Control microoperations, execution of a complete instruction.

Microprogrammed control, encoding of control signals, microprogram sequencing, hardwired control, basic control of a MIPS instruction set.

Pipelined datapath, data hazards, data forwarding, stalling, branch hazards.

**Date and Location for Exam**

Wednesday, March 9, 2005.
Location: 1221 CS
Time: 7:15 pm to 9:15 pm.
Duration: 2 hours

**Copies of old exams are available on line**.

**Exam is CLOSED book and notes. No crib sheet allowed.**