Compiling and Simulating VHDL at CS

CS/ECE 552-2
Fall 1998

To Set Up for VHDL: (done one time)

1. cd $MGC_WD
   This is your main Mentor Graphics directory.
2. mkdir vhdlcode
   This creates the directory in which you will place your VHDL source code.
3. mkdir vhdlsym
   This creates the directory in which you will place your VHDL symbols, created in Design Architect.
4. qhlib vhdllib
   This creates the directory that will contain the library of all VHDL devices that you create. When you compile a device's VHDL description, the result will be placed here.
5. qhmap vhdl552 $MGC_WD/vhdllib
   This tells Mentor to look in the directory that you created in step 4 to find the model information for your devices. You will refer to this model library as "vhdl552."

To Create and Compile a VHDL File:

1. cd $MGC_WD/vhdlcode
2. Create <yourfile>.vhdl using your preferred text editor.
3. qvhcom <yourfile>.vhdl -work vhdl552 -qhpro_syminfo
   This compiles the device and places the working model in the library called "vhdl552."
4. Fix any errors and repeat step 3.

To Generate a Symbol for the New Device in Design Architect:

1. da
   This starts Design Architect.
2. File->Generate->Symbol
   This brings up the symbol creation dialog box. Fill it in with:
   Choose source: Entity
   Library Logical Name: Choose Library->vhdl552
   Entity Name: Choose Entity-> <your new device>
   Default Architecture: Choose Arch-> <your architecture>
   Directory: $MGC_WD/vhdlsym
   Click "OK"
3. Check and save the symbol.

To Create a Schematic that Uses the New Symbol:

Open a new schematic in Design Architect and click on "Choose Symbol" in the "Schematic: Add/Route" window on the right to add it to the schematic. This creates <schematic dir> as mentioned below.

To Simulate a Design that has VHDL Objects:

1. `cd $MGC_WD`
2. `qhpro <schematic dir> -lib vhdl552`
   This starts QuickSim II. Be sure to start it this way and not directly. If you start it directly, you will get “model not found” warnings for your devices, since their models are found in “vhdl552,” and attached by QhPro.
3. `Solver->QuickSim II`
   This menu selection is on the far right.

You can now simulate the design in the normal way. Ignore the additional window that came up.

To Invoke a Force File on this Design:

1. `File->Open Sheet`
   This opens a window with the design that you are simulating. You do not have to do this, but it makes the trace window more meaningful if you can see the design.
2. `Setup->Force->From file...`
   This allows you to select the force file that you want to apply to this circuit.

To Simulate a VHDL file only:

1. `cd mentor`
2. `qhsim -lib vhdllib`
3. Select your design.
4. `type view *`

You do not need to use this simulator. It’s for people who want to simulate their VHDL, but don’t want to wait for QhPro to start. You are on your own to figure out how to use it.