Somayeh Sardashti

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Research Interests

My research areas of interest are computer architecture, in particular energy-efficient processor designs and memory hierarchies.

Education

Doctorate of Philosophy in Computer Sciences **Summer 2014**
Supervisor: Professor David A. Wood
Computer sciences department of University of Wisconsin-Madison
GPA: 4.0/4.0

Masters of Science in Computer Science **May 2011**
Supervisor: Professor David A. Wood
Computer sciences department of University of Wisconsin-Madison
GPA: 4.0/4.0

Masters of Science in Computer Engineering **February 2006**
Electrical and Computer Engineering Department of University Of Tehran
GPA: 18.69/20.00 (graduated with highest honor)

Bachelor of Science in Computer Engineering **September 2003**
Electrical and Computer Engineering Department of University Of Tehran
GPA: 17.66/20.00 (graduated with highest honor)

Skills

C, C++, Python, Assembly, Verilog, VHDL, Cadence and Synopsys EDA tools, LINUX, Windows, GEM5 and GEMS full system simulators, and SimpleScalar.

Work and Research Experiences

9/2008-Present PhD Candidate, UW-Madison, WI, Multifacet Group

- Contributed on writing NSF technical proposal "Energy-Optimized Memory Hierarchies".
- Investigating techniques for energy-optimized memory hierarchies in multi-core processors.
- Investigating techniques to improve performance, bandwidth, and energy-efficiency of die-stacked DRAM caches.
- Improving compression effectiveness for energy-efficiency by exploiting spatial locality.

- Studying compression effectiveness for different server and commercial workloads.
- Investigating techniques for low-complex compressed caching (in collaboration with Professor Andre Seznec from IRISA/INRIA).
- Developed a unified technique for fault-tolerance and idle power management of large multi-core systems by exploiting non-volatile memory technologies.
- Contributed in development of gem5 full system simulator.
- System administrator of Multifacet Solaris machines.
- System administrator of Multifacet storage.
- Some of the course projects:
    - Implemented and evaluated IBM POWER6 coherence protocol using GEMS.
    - Applied ACE analysis on a superscalar processor using SimpleScalar.
    - Developed a MIPS-like multi-cycle processor from high level design to layout extraction, including a full-custom 32x16 cell SRAM.
    - Parallelized x264 encoder with TBB and PThread by leveraging Intel VTune.
    - Used analytical models to understand and model power savings in servers while applying different idle power management techniques.

5/2011-09/2011 Intern, AMD Boston Design Center
- Studied energy efficiency of cache prefetchers in AMD next generation processors under supervision of Dr. John Kalamatianos.

5/2007-8/2008 Hardware Engineer, University of Tehran, Iran
- Contributed in system level design of a hardware-based H.264 encoder.
- Designed and implemented different components of H.264 encoder such as Interpolation and Fractional Motion Estimation Units.

3/2006-4/2007 Design Engineer, SiNA Semiconductor Co. Iran
- Contributed in system level test and verification of a Broad Band Gateway.

9/2004-2/2006 Research Assistant, University of Tehran, Iran
- Designed and implemented a Multi-threaded Stream processor for Media applications as my Master thesis.
- Developed a cycle-accurate simulator for a Multi-threaded Stream processor.
- Designed and implemented a Multi-threaded Stream processor at RTL level.

9/2003-9/2004 Research Assistant, University of Tehran, Iran
- Contributed in developing a tool for converting Verilog codes to SystemC.

Teaching Experiences

9/2008-4/2009 Teaching Assistant, UW-Madison, WI
- "Machine Organization and Programming" for three semesters.
    - Lectured in the class, graded exams and homework.
- "Introduction to Computer Architecture" for one semester.

- Helped students for their class projects, setting up simulation and synthesis tools, debugging their Verilog codes, etc.
- Developed a cache simulator that has been actively used in this since then (http://pages.cs.wisc.edu/~david/courses/cs552/S12/includes/cache-sim.html).

05/2002-11/2004 Teaching Assistant, University of Tehran, Tehran, Iran

- "Design of Digital Systems with VHDL" for one semester.
  - Designed homework and exams in addition to grading.
- "Digital Logic Circuit Laboratory" for three semesters.
  - Lab instructor, teaching students to build hardware prototypes using FPGA and TTL.
- "Introduction to Computer Architecture" for two semesters.
  - Mentored several students for their class projects.

Service and Professional Activities

2010-Present Mentoring Chair of UW-Madison ACM-W (WACM)

- Organized and hosted several speaker series, invited technical women from Oracle, Google, Microsoft, etc.
- Mentoring several female undergraduate students to pursue careers in Computer Sciences.

Fall 2012-Spring2013 Scratch Club Leader, Madison, WI

- Volunteered at an after-school club for elementary school students to teach them the basics of programming in Scratch.
- Volunteered at the scratch class of UW Grandparents University.

2010-2013 Founder and Officer of UW-Madison Persian Student Society

Peer Reviewer for IEEE Transactions on Computers

2009 Graduate Admissions Committee, University of Wisconsin–Madison

Honors

- Winner of Graduate Network Peer Mentor Awards, UW-Madison, 2014.
- One of the seven finalists out of over 360 disclosures in WARF (Wisconsin Alumni Research Foundation) innovation awards, 2013.
- First place in ACM Student Research Competition at the ACM-W Grace Hopper Celebration, 2013.
- Ranked 1st in the graduate program, Computer Architecture Engineering, University of Tehran, 2006.
- Ranked 28th in National Graduate Entrance Exam among 5,000 competitors, 2003.
- Ranked 3rd in the undergraduate Program, Computer Engineering, University of Tehran, 2003.
- Ranked 219th in National Undergraduate Entrance Exam among 300,000 competitors, 1999.

Publications

- **S. Sardashti**, and D. Wood, " Decoupled Compressed Cache: Exploiting Spatial Locality for Energy Optimization, " IEEE Micro Top Picks in Computer Architecture, 2014.
- **S. Sardashti**, and D. Wood, " Decoupled Compressed Cache: Exploiting Spatial Locality for Energy-Optimized Compressed Caching, " The 46th Annual IEEE/ACM International Symposium on Microarchitecture, 2013.
- **S. Sardashti,** "Exploiting Spatial Locality for Energy-Optimized Compressed Caching," **Winner of ACM Student Research Competition**, ACM-W Grace Hopper Conference, 2013.
- **S. Sardashti**, and David Wood, " UniFI: A Unified Fault Tolerance and Idle Power Management Technique, " 26th International Conference on Supercomputing (ICS), 2012.
- N. Binkert, B. Beckmann, G. Black, S. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. Hower, T. Krishna, **S. Sardashti**, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. Hill, and D. Wood, "The gem5 Simulator," SIGARCH Computer Architecture News, 2011.
- N. Binkert, B. Beckmann, G. Black, S. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. Hower, T. Krishna, **S. Sardashti**, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. Hill, and D. Wood, "gem5: A Multiple-ISA Full System Simulator with Detailed Memory Model", ISCA workshops and tutorials, June 2011.
- **S. Sardashti**, H. Ghasemi, M. Semsarzadeh and M. Hashemi, "High Performance Mathematical Quarter-Pixel Motion Estimation with Novel Rate Distortion Metric for H.264/AVC," published by Springer's Communications in Computer and Information Science (CCIS) series, 2008.
- **S. Sardashti**, H. Ghasemi and O. Fatemi, "MISP: Multithreaded multi Issue VLIW Stream Processor," Proc. of IEEE International Conference on Multimedia and Expo (ICME'06), Toronto, July 2006.
- **S. Sardashti**, H. Ghasemi and O. Fatemi, "MVSP: Multithreaded VLIW Stream Processor," Proceedings of the IS&T SPIE Electronic Imaging (EI '06), January 2006.
- B. Robatmili, N. Yazdani, **S. Sardashti**, M. Nourani, "Thread-Sensitive Instruction Issue for SMT Processors," IEEE Computer Architecture Letters, Volume 3, Aug. 2004.
- C. Rubio-González, I. Burcea, R. Enciso, **S. Sardashti**, and Y. Watanabe. "Conference Networking Across Boundaries". Grace Hopper Celebration of Women in Computing (GHC'10), Birds of a Feather (BoF), Atlanta, GA.

Patents

- **S. Sardashti**, D. Wood, "Energy Optimized Cache Memory Architecture Exploiting Spatial Locality," Filed October 2012, US Patent Pending, 1512.432: P130076. **One of the seven finalists (out of 360 disclosures) in WARF innovation awards.**