Sujay Yadalam

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RESEARCH INTERESTS

Computer Architecture, Persistent memory, Hardware security, Big Data systems

EDUCATION

UNIVERSITY OF WISCONSIN-MADISON | MS, PhD in Computer Science — August 2019 - Present
GPA: 3.89/4.0
Courses: Introduction to Operating Systems, Advanced Computer Architecture I, Advanced Computer Architecture II, Next Generation Databases, Advanced Machine Learning, Big Data Systems, Distributed Systems, Algorithms

PES UNIVERSITY | B.E in Electronics and Communication — August 2012 - May 2016 | Bangalore, India
GPA: 9.54/10 | Rank: 11 out of 141 students

PUBLICATIONS

[1] Yadalam, Sujay, Vinod Ganapathy, and Arkaprava Basu. "**SGXL: Security and Performance for Enclaves Using Large Pages.**" ACM Transactions on Architecture and Code Optimization (TACO) 18, no. 1 (2020): 1-25

RESEARCH EXPERIENCE

WISCONSIN MULTIFACET PROJECT | Research Assistant — January 2020 - Present | UW Madison
Advisor(s): Prof. Michael Swift & Prof. Xiangyao Yu

- Studied architectures and systems that can provide efficient access to Persistent memory to improve the performance of recoverable applications with in-memory data structures.
- Developed an architecture that performs significantly better than currently available systems. Proposed design involves modifications to the cache subsystem and the memory controllers to reduce the number of stalls and improves the bandwidth utilization.

Persistent Memory | Architecture | Caches | Memory Controller | gem5

VMWARE RESEARCH GROUP | Research Intern — June 2021 - September 2021 | Palo Alto
Advisor(s): Jayneel Gandhi

- Rethinking software and hardware stack to achieve low latency accesses to NVMe devices.
- Developed a design to achieve low cost in-core communication across privilege levels.

Storage technologies | NVMe | Privilege mode switches

COMPUTER SYSTEMS LAB | Research Assistant — August 2018 - July 2019 | Indian Institute of Science
Advisor(s): Prof. Arkaprava Basu & Prof. Vinod Ganapathy

- Studied hardware side channel attacks and defences against them. Studied trusted execution environments and their weaknesses.
- Developed a software-hardware defence for page-access based side channel attacks against the Intel® SGX. Proposed solution includes minor hardware enhancements and modifications to the SGX SDK and SGX driver (Linux kernel module).

Hardware Security | Intel® SGX | Side-channels | Linux kernel | CACTI (Cache modelling)

REVERSIBLE COMPUTING LAB | Undergrad Researcher — Jan 2015 – May 2016 | PES University
Advisor(s): Prof. Jayashree.H.V

- Focused on design and analysis of Reversible datapath subsystems with primary focus on reversible binary comparators.
- Designed an Ancilla-invariant reversible binary comparator with performance parameters comparable to existing designs.

Reversible computing | Binary comparators | Verilog | ISE simulator

INDUSTRIAL EXPERIENCE

CYPRESS SEMICONDUCTOR | Applications Engineer — July 2016 - July 2018 | Bangalore, India

- Worked on the Bluetooth stack, mostly on the power management module.
- Developed an Indoor Positioning System based on Bluetooth Low Energy for demonstration purposes.

ANALOG DEVICES | Co-op Intern — Jan 2016 - Jun 2016 | Bangalore, India

- Analyzed performance of different embedded micro-processors for mathematical and DSP algorithms by using trace driven methodologies. The results of the analysis were utilized to optimize algorithms.

RESEARCH PROJECTS

ACCELERATING DATABASE ANALYTICS — Spring 2020 | UW Madison

- Developed a CPU-GPU database system that addresses the memory constraints on the data residing in the accelerator's memory. Unlike prior work, the proposed system does not limit the size of the database that a GPU can work on.
- The design involved smart data placement and task scheduling to improve the performance of in-memory analytics. Performance was evaluated using Star Schema Benchmark on a NVIDIA Pascal P100 GPU.

Data analytics | Heterogeneous database | Device memory | Star Schema benchmark | CUDA

REGISTER CACHING IN GPUS — Sprint 2020 | UW Madison

- Studied the impact of register caching in GPUs. Register caches can improve the overall register file capacity without adversely affecting the access latencies and energies.
- Our experiments revealed that register caching can improve SM occupancy, thereby improving the performance. However register caches suffers from a high miss rate. To mitigate this, we proposed a hardware prefetcher that loads registers into the register cache asynchronously.

GPU register file | Caching | SM occupancy | gpgpu-sim

NO MORE TLB LEAKS! — Fall 2019 | UW Madison

- Similar to caches, Translation Lookaside Buffers(TLB) are vulnerable to timing side-channel attacks. Developed a new TLB design dubbed RPTLB (Random Prefetching TLB) that defends against these side-channel attacks.
- Proposed solution uses random prefetching to obfuscate a victim's page access pattern from an attacker.

Hardware security | Side-channels | TLBs | Prefetching

FRACTAL BASED DEVICE STRUCTURES IN ELECTRONIC DESIGN — Jan 2016 - May 2016 | PES University

- Studied fractal structures in electronic design such as fractal antenna, capacitors and inductors.
- Designed and analyzed IC resistors modeled using Hilbert and Peano curves. Also derived empirical formulae for the same.

TEAM HAYA RACING | Electrical Subsystem Member — Aug 2013 - May 2016 | PES University

- Designed the electrical circuit for the racecar and configured the engine sensors and actuators.
- Performed engine tune-up and created the fuel and ignition maps for the engine.
- Designed servo based paddle shifter.
- Developed a hall-sensor based speedometer, utilized by the ECU for launch control.

LANGUAGES AND TOOLS

PROGRAMMING LANGUAGES

Over 5000 lines: C, C++ • Python
Over 500 lines: CUDA • Java • MATLAB • Verilog

TOOLS/FRAMEWORKS

gem5 | gpgpusim | CACTI | Linux