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AutoMapper – An Automated Tool for Optimal Hardware Resource Allocation for Networking Applications on FPGA*

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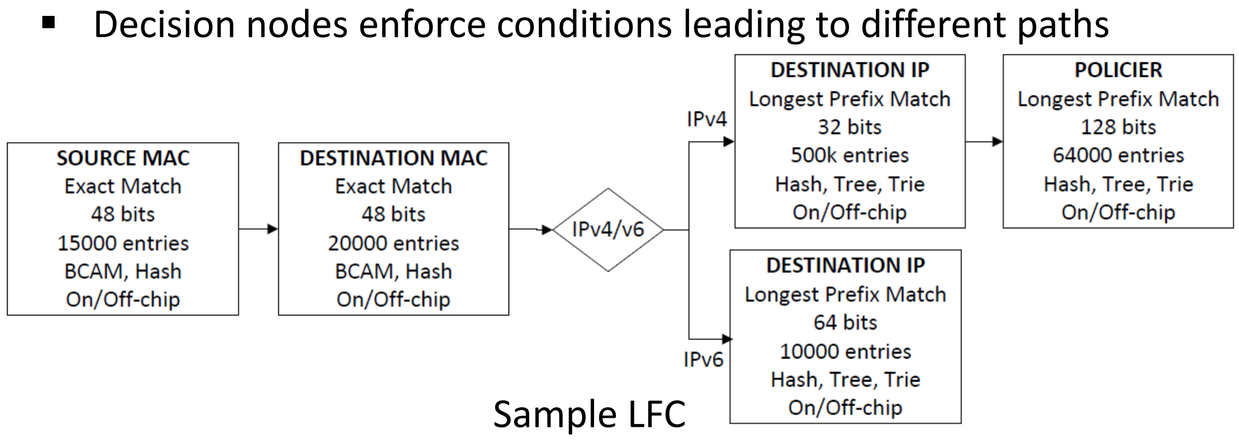
Introduction

- Ethernet/IP based packet forwarding
  - Complex sequences of lookup operations
  - High throughput, low latency and power consumption desired
  - Need efficient resource utilization of hardware
- Field Programmable Gate Arrays
  - Ideal choice for high-performance networking applications
  - Parallelism, reconfigurability and the abundant on-chip resources
  - Supports efficient implementations of packet lookup engines.

Background

- Lookup Scheme Representation
  - Lookup Flow Graph
  - Sequential arrangement of field nodes
  - Field nodes depict distinct lookup operations
  - Decision nodes enforce conditions leading to different paths

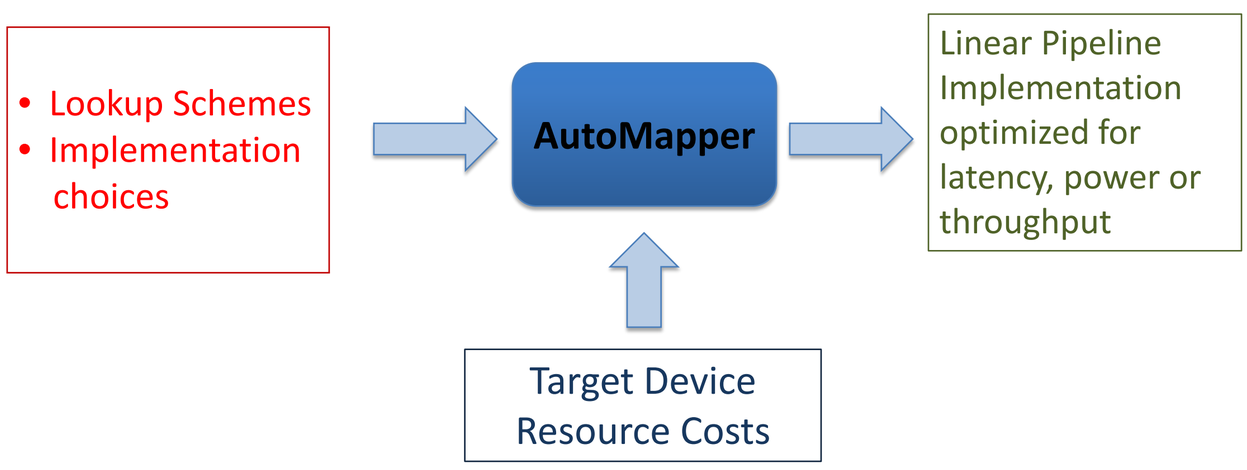


Sample LFC

Challenges

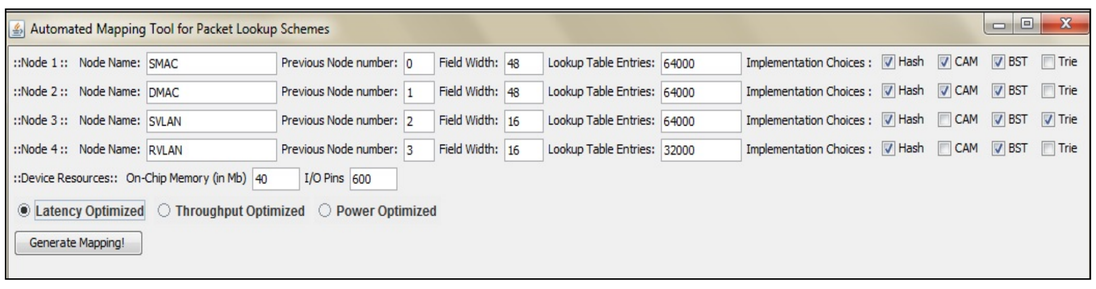
- Mapping Problem
  - Generation of a linear pipeline architecture
  - Incorporating all lookup operations in a LFG
  - Optimizing power, throughput or latency
- Ineffective Manual Organization Techniques
  - No guarantee of optimality
  - Time-consuming
  - Wasteful allocation of target resources
  - Difficult to calculate resource costs and latency

Tool Features



Key Ideas

- Generates input LFG structure
- Identifies distinct paths and location of decision nodes
- Computes the resource costs of implementation choices
- Creates an ILP formulation, corresponding to the mapping problem
- Interprets the optimal solution
- Generates the high- level mapping



AutoMapper Screenshot

Experiments

Table 1: Details about Sample Lookup Schemes

S.No.	Field Nodes	Decision Nodes	Field Width	Table Size
I	4	0	16-48	64k-256k
II	6	0	16-48	32k-100k
III	6	1	20-128	64k-128k
IV	7	1	16-128	4k-256k
V	7	2	20-128	64k-128k

Lookup Scheme	Latency-optimized	Throughput-optimized		Power-optimized	
	Latency#	Latency#	Pipelines per chip	Latency #	Dynamic Power*
Scheme I	5	38	7	66	0.076479
Scheme II	7	69	5	95	0.083168
Scheme III	8	135	4	179	0.155098
Scheme IV	15	231	4	416	0.037949
Scheme V	10	199	4	241	0.156077

In terms of clock cycles
* As fraction of the dynamic power in the latency-optimized case

Conclusion

✓ Automapper- automated tool
- Optimally maps complex lookup schemes onto FPGAs
- Maps on to a linear pipelined architecture
- Optimizes for latency, power or throughput

Future Work

- Extend the tool
  - Generate a synthesized implementation for the mapped pipeline in HDL
  - Incorporate mapping of multiple LFCs simultaneously

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