

# A 0.4V 7T SRAM with Write Through Virtual Ground and Ultra-fine Grain Power Gating Switches

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**Abstract**—This paper presents a 7T near-threshold SRAM with design techniques for improving cell stability and energy efficiency. The proposed write through virtual ground (WTVG) scheme decreases the period of write disturbance by  $6.1\times$ . A PVT tracking sensing scheme is presented to track variation and sense small RBL swing. The ultra-fine grain power gating switches are implemented to minimize the redundant leakage caused by the storage of garbage data. The leakage suppression of 52% is achieved after the initial power-up. A 16 kb SRAM test chip was fabricated in a 65nm CMOS technology and showed the minimum energy of 2.01 pJ at 0.4 V.

## I. INTRODUCTION

Ultra-low power circuits are strongly required in extensive applications such as intelligent mobile phones, hand-held entertainment devices, BAN (body area network) sensor nodes, etc [1],[2]. Near-threshold or sub-threshold CMOS circuits play a critical role in these applications where power consumption reduces significantly due to their exponentially decreased current with supply voltage scaling in weak-inversion region [3]. As a major memory component, SRAMs occupy large area and dissipates high energy in system-on-chips (SoCs). In the near-threshold or sub-threshold region, conventional 6T SRAMs are not reliable due to severely degraded cell stability including half-selected problem, poor bitline sensing margin, and exponentially increased sensitivity to PVT (Process, Voltage and Temperature) fluctuations. Therefore, conventional 6T SRAM cells cannot facilitate reliable operation with high density and high yield [4].

Decoupled SRAM cells have been verified to work in the sub-threshold or near-threshold region [5-9]. While decoupled SRAM cells improve the cell stability substantially during read operation, the stability of the half-selected cells is still a challenging issue. Pulsed wordlines and hierarchical bitlines [10] mitigate the stability degradation of the half-selected cells, but they degrade the write margin, demanding write margin improvement techniques. Therefore, design parameters and assisting circuits have to be carefully selected by trade-offs. In ultra-low voltage SRAMs, leakage current occupies a substantial percentage of power and energy. Thus, energy-aware leakage reduction is also important for the better energy efficiency.

In this paper, we present an area efficient 7T SRAM with various circuit techniques: (i) a single-ended 1T read port for minimizing SRAM cell area overhead, (ii) PVT tracking reference generator for sensing small RBL swing, (iii) write through virtual ground (WTVG) scheme for improving stability, and (iv) ultra-fine grain power gating (UFG) switches for redundant leakage reduction.

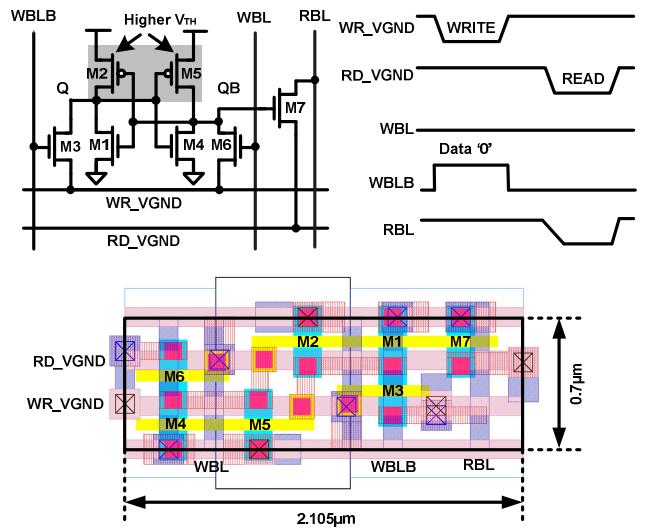


Figure 1. Proposed 7T SRAM cell and read/write operations.

## II. PROPOSED 7T SRAM CELL

The proposed 7T SRAM cell and its operation are depicted in Fig. 1. Higher-V<sub>th</sub> devices are employed in the pull-up PMOS transistors (M2 and M5) to improve the write margin and reduce the leakage. A single-ended 1T read port is proposed for minimizing area overhead. This is achieved by removing the read access transistor in the traditional 8T SRAM cell [1]. When read is enabled (RD\_VGND = GND), the precharged read bitline (RBL) is conditionally discharged by QB. When QB = '1', the pull-down cell current fights with the pull-up leakage current from unselected RD\_VGNDs through M7, resulting in DC offset in the level of data '0'. However, in the near-threshold region, the DC offset imposes body effect on M7 in unselected rows and M7 operates in the sub-threshold region. Through this, the RBL swing becomes large enough to be sensed without the access device in [1]. During non-read cycles, RD\_VGND and RBL are held to VDD, thus removing the bitline leakage through M7. Write operation starts by applying GND to WR\_VGND and loading write data in the write bitlines (WBL and WBLB). One of M3 and M6 will be writing '0' into the selected node. In unselected rows, WR\_VGND becomes floating after precharged at VDD. Due to the small loading at WR\_VGND, disturbing current flows only for a short time. In unselected columns, both WBL and WBLB are GND, and prevent the conventional half-select issue. The layout size of the SRAM cell is  $2.105 \times 0.7 \mu\text{m}^2$  using the logic design rule.

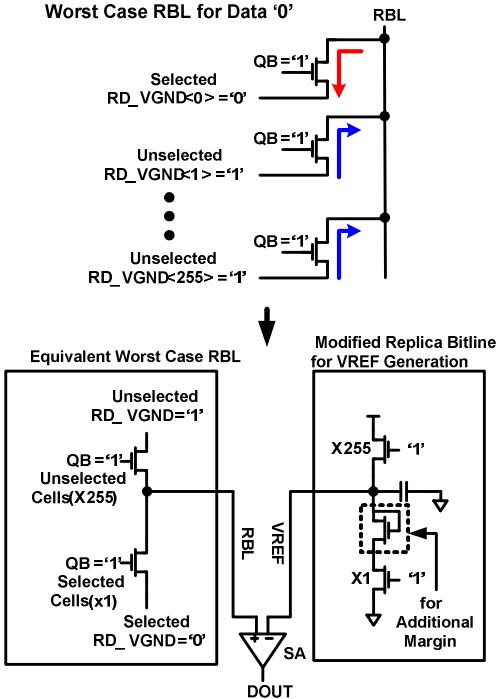


Figure 2. A PVT tracking reference generator using a modified bitline replica.

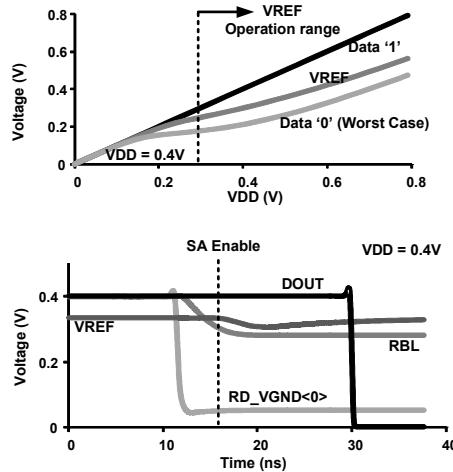


Figure 3. Simulation results of small bitline sensing of the worst case read.

### III. PROPOSED ULTRA-LOW VOLTAGE SRAM TECHNIQUES

#### A. Bitline Sensing with PVT Tracking Reference Generator

The worst case read is illustrated in Fig. 2. The worse case RBL for data '0' is formed at a level where the pull-up strength through the unselected cells is balanced to the pull-down strength through the selected cell. Increasing the number of cells per bitline will raise the offset for data '0'. The offset of 0.28 V was observed with the supply voltage of 0.4 V and 256 cells per bitline. Simple inverters will fail to sense this small RBL swing. Differential sense amplifiers with a PVT tracking reference generator (Fig. 2) are developed to sense the small RBL swing. A modified replica bitline automatically tracks the device variations and provides VREF with a margin

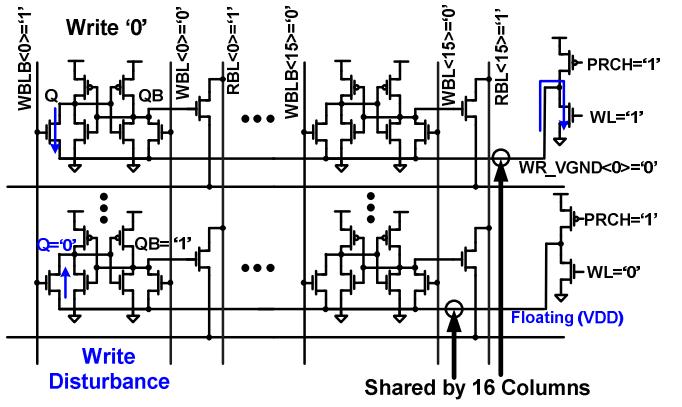


Figure 4. Write disturbance occurring in a column.

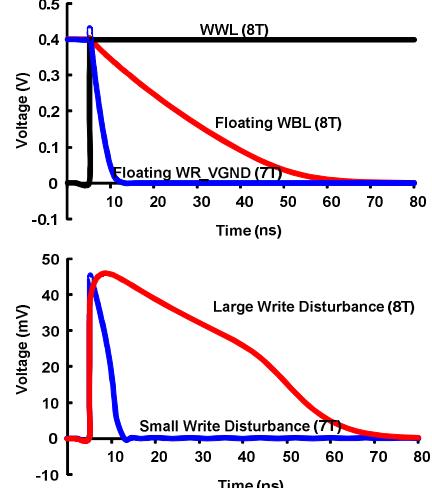


Figure 5. Improved stability by small capacitance and fast discharging.

controlled by the strength of the diode. Fig. 3 demonstrates the simulation results of the worst case RBL read and VREF generation. Simulation verifies that the VREF generator provides enough margin by the diode for both data '1' and '0' over a wide operating range. The VREF is 0.34 V at the supply voltage of 0.4 V, enough to sense the RBL swing with the DC offset of 0.28 V.

#### B. Write Through Virtual Ground Scheme

In the proposed SRAM array, the unselected cells in the selected row are free of disturbing due to their grounded WBLs/WBLBs. But the unselected cells in the selected column still have a disturbing condition as shown in Fig. 4. For example, a write operation is executed to the cell located at the first row and the first column. WR\_VGND<0> is grounded while other WR\_VGNDs are all floating. The write driver loads data '0' to the first column, making WBL<0> = '0' and WBLB<0> = '1'. For the cell of Q = '0' along the WBLB<0>, disturbing current flows from floating WR\_VGND (e.g. WR\_VGND<255>) to Q node (Fig. 4). However, compared to the conventional SRAM cells, the write disturbance in the proposed cell (Fig. 5) is remarkably ameliorated by the smaller parasitic capacitance. Conventional write disturbance is determined by capacitance at WBL/WBLB while the proposed one depends on the capacitance at WR\_VGND. Since the number of devices

connected to WR\_VGND is much smaller than that of conventional bitlines, floating WR\_VGNDs are quickly discharged and accordingly improve the dynamic cell stability as illustrated in Fig. 5. Although the peak values of disturbance are similar, the disturbing duration of the 8T SRAM is as large as  $6.1\times$  that of the proposed SRAM. Similarly, floating WR\_VGND is also discharged within 6× faster than that of 8T SRAM at 0.4 V. Therefore, dynamic cell stability is enhanced by the write through virtual ground technique. Moreover, the number of error bits by write disturbance is limited to one out of a row. Therefore, any error caused by write disturbance in this 7T work could be easily corrected via simple checking methods such as parity check.

#### IV. ULTRA-FINE GRAIN POWER GATING SWITCHES

In many ultra-low energy systems, unwanted power dissipation occurs due to the cells storing invalid data and the frequent dynamic voltage scaling. The proposed ultra-fine grain power gating switches minimizes the leakage and wake-up current of the SRAM cells with garbage data. Fig. 6 illustrates the architecture of the proposed power gating switches. A column of VDD switches controls each row while a row of VSS switches manages each column. The switches in each row and column will be on when a row and a column is accessed for the first writing. The power switches of the unaccessed rows and columns are off, consequently suppressing the leakage and the peak current during subsequent power-up.

The schematics of the power gating switches are described in Fig. 7. To utilize the power gating switches without complex control circuits, the power switches have to be automatically in the off-state after a power-up. An HVT (High Threshold Voltage) PMOS transistor is added between M3 and M4 to make Q0 rise slower than Q1 by reducing the power-up current through M3. An initial power-up will initialize Q0 with ‘0’ and Q1 with ‘1’ (off-state) turning off M1 and M2 in Fig. 7(a), and M9 in Fig. 7(b). The strength of M7 was verified by Monte Carlo simulation ( $n=1000$ ). When the first write operation is asserted, WL and COL of the selected row and column write data ‘0’ into Q1 (on-state) and enable the power gating switches. Note that each SRAM cell has two VDD rails shared by neighboring cells. Thus each VDD switch has two switches. The VDD switches and the VSS switches are placed perpendicularly, generating 4

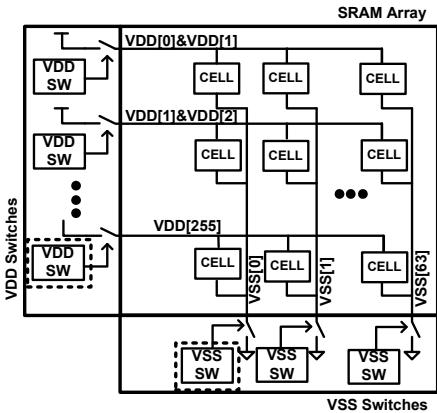


Figure 6. Architecture of ultra fine power gating switches.

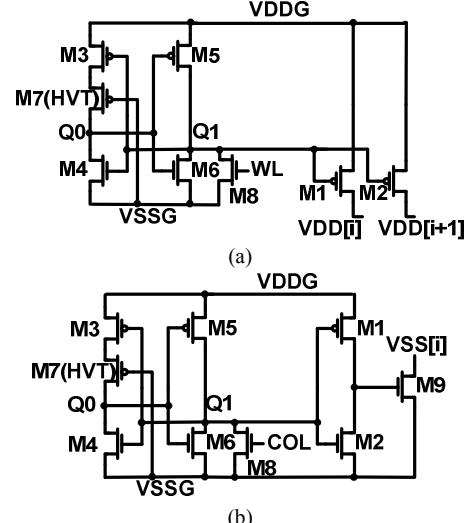


Figure 7. Schematics of the proposed power gating switches: (a) VDD switch and (b) VSS switch.

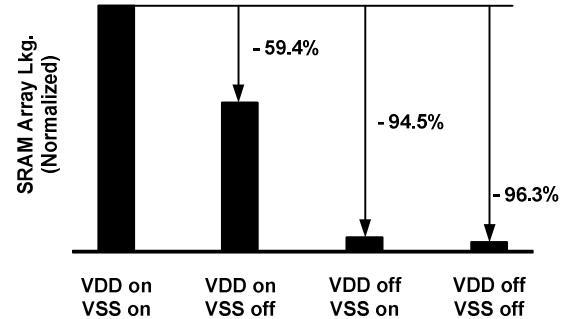


Figure 8. Summary of leakage reduction from the proposed power gating.

different power gating scenarios in each cell (Fig. 8). Maximum reduction will be achieved from the cells where the VDD switch and the VSS switch are off while mitigated reduction can be achieved when one of the VDD and VSS switches is on. Simulation shows that the SRAM array achieves the initial leakage saving of 96.3% after power-up. As the portion of accessed cells increases, the savings decrease to 0% (VDD on, VSS on). The area overhead caused by the ultra-fine grain power gating switches is controlled within 2.4% for the VDD switches and 2% for the VSS switches.

#### V. TEST CHIP MEASUREMENT

A 16kb SRAM test chip was fabricated in a 65nm CMOS technology (Fig. 10). The SRAM array is organized with 256 rows × 64 columns. Each write virtual ground (WR\_VGND) is shared by 16 columns while RD\_VGND is shared by the whole 64 columns. Fig. 9 demonstrates the leakage, energy, power, and performance measurement results. The leakage current decreases from 64  $\mu$ A to 1  $\mu$ A by lowering VDD from 1.2 V to 0.25 V (27°C). The measured average power is 0.625  $\mu$ W at 0.25 V and 13.44  $\mu$ W at 0.4 V, respectively. The read power is larger than the write power due to the static leakage current in the read bitline during read operation. The SRAM has the minimum energy of 2.01 pJ at 0.4 V. The test chip is functional down to 0.25 V with the maximum operating

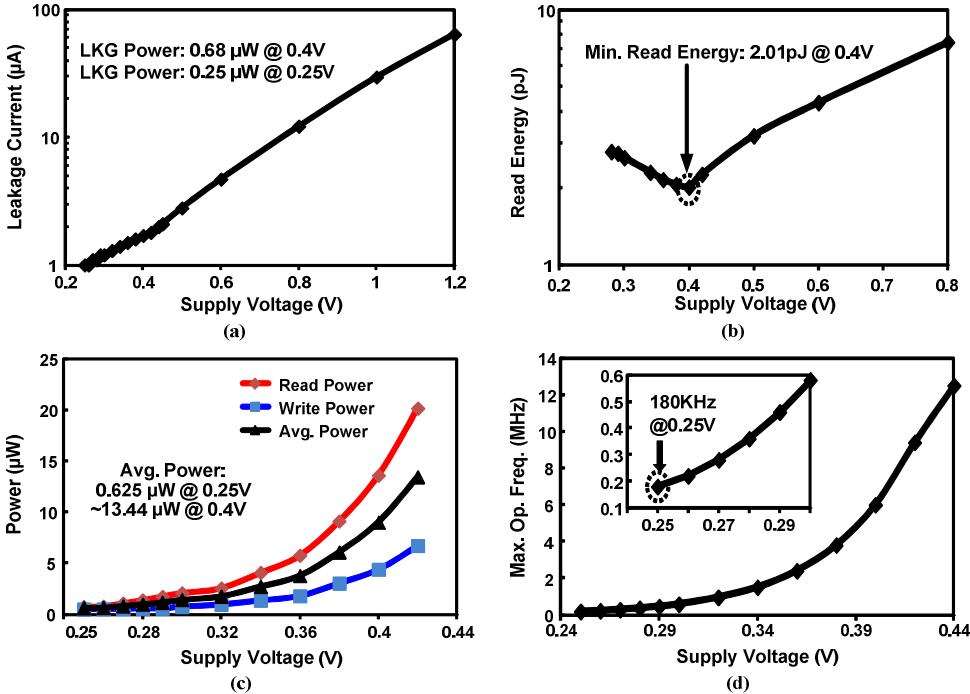


Figure 9. Measurement results: (a) leakage current, (b) read energy consumption, (c) power consumption, and (d) maximum operating frequency.

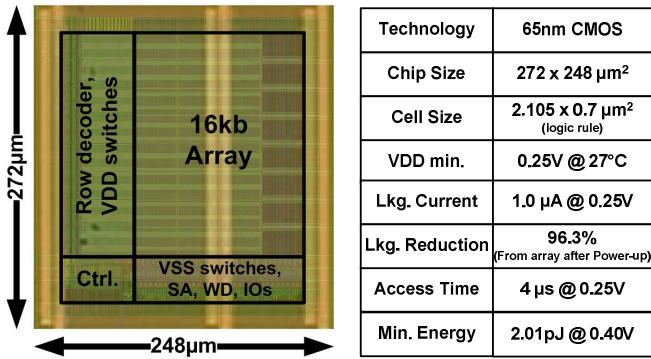


Figure 10. Chip micrograph and summary.

frequency of 180 kHz (27°C). The read access time maintains at 4  $\mu\text{s}$  at 0.25 V. The SRAM test chip achieves the leakage reduction of 52 % after the initial power-up at 1.2V.

## VI. CONCLUSION

A 0.4 V, 2.01 pJ 7T SRAM with write through virtual ground (WTVG) and ultra-fine power gating switches is presented. The 1T based read port improves array area efficiency compared to the conventional 8T SRAM cell. The PVT tracking VREF generator enables the sensing of smaller bitline swing caused by the 1T read port. WTVG scheme is proposed to improve the dynamic cell stability by shortening time of disturbance through short virtual ground. Ultra-fine grain power gating switches are developed to suppress leakage of SRAM array after power-up. The power gating switches reduced the leakage current by 52% after power-up. The test chip measurement shows that the proposed circuit techniques can be employed in numerous ultra-low power applications requiring ultra-low voltage operation.

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## REFERENCES

- [1] K. Song, et al., "A 20 $\mu\text{W}$  contact impedance sensor for wireless body-area-network transceiver", IEEE Custom Integrate Circuit Conference, September 2011.
- [2] B David, et al., "A 25MHz 7 $\mu\text{W}$  Ultra-low-voltage Microcontroller SoC in 65 nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes", ISSCC, pp. 490-491, February 2012 ,
- [3] H. Soeleman, et al., "Robust Subthreshold Logic for Ultra-Low Power Operation", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 9, No. 1, pp. 90-99, February 2001.
- [4] T. Kim, et al., "A Voltage Scalable 0.26 V, 64 kb 8T SRAM With Vmin Lowering Techniques and Deep Sleep Mode", IEEE Journal of Solid-State Circuits, Vol. 44, No. 6, June 2009.
- [5] C. Leland, et al., "A 5.3GHz 8T-SRAM with Operation Down to 0.41V in 65nm CMOS", Symposium on VLSI Circuits, pp. 252-253, June 2007.
- [6] S. Yoshimoto, et al., "A 40-nm 0.5-V 20.1- $\mu\text{W}/\text{MHz}$  8T SRAM with Low-Energy Disturb Mitigation Scheme", Symposium on VLSI Circuits, pp. 73-74, June 2011.
- [7] M. Chang, et al., "A 130 mV SRAM With Expanded Write and Read Margins for Subthreshold Applications", IEEE Journal of Solid-State Circuits, Vol. 46, No. 2, February 2011.
- [8] T. Kim, et al., "A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme", ISSCC, pp. 330-331, 607, February 2007.
- [9] J. Wu, et al., "A Large  $\sigma_{V_{TH}}/\text{VDD}$  Tolerant Zigzag 8T SRAM With Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme", IEEE Journal of Solid-State Circuits, Vol. 46, No. 4, April 2011.
- [10] K. Takeda, et al., "Multi-step Word-line Control Technology in Hierarchical Cell Architecture for Scaled-down High-density SRAMs", Symposium on VLSI Circuits, pp. 101-102, June 2010.