

# Zuyu (Anthony) Zhang

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EDUCATION	<b>Ph.D. Candidate, Database Systems</b> 2012-2017 (Expected) University of Wisconsin-Madison, Madison, WI, USA Advisor: <b>Prof. Jignesh Patel</b> Thesis topic: Towards high perf., cloud-based distributed analytical query processing.
	<b>M.Eng., Computer Systems Organization</b> 2010-2012 Harbin Engineering University (HEU), Harbin, China Thesis: LLVM Back-end Porting for C*Core Architecture.
	<b>B.Eng., Computer Science and Technology</b> 2006-2010 Harbin Institute of Technology (HIT), Harbin, China
TECHNICAL SKILLS	Prog. Lang.: C/C++, BASH scripting, and X86 assembly. Tools: LLVM, gFlags, gLog, gTest, CMake, Bazel, Protobuf, gRPC, GIT, and L <sup>A</sup> T <sub>E</sub> X.
EXPERIENCE	<b>Software Engineering Intern, Google</b> Oct-Dec 2016 <ul style="list-style-type: none"><li>Working on multi-tenant, interactive reporting service in C++.</li></ul>
	<b>Software Engineering Intern, Twitter</b> Jul-Sep 2016 <ul style="list-style-type: none"><li>Exploited streaming query execution on Twitter Heron.</li></ul>
	<b>Software Engineering Intern, Pivotal</b> Jun 2015-Jul 2016 <ul style="list-style-type: none"><li>Research and develop distributed analytical SQL query processing techniques.</li></ul>
	<b>Core Team Member, Quickstep Technologies</b> Jan-Jun 2015 <ul style="list-style-type: none"><li>Spinoff from the <b>Quickstep</b> project at UW-Madison, and acquired by Pivotal.</li></ul>
	<b>Software Engineering Intern, Twitter</b> May-Aug 2014 <ul style="list-style-type: none"><li>Prototyped Twitter Heron Scheduler on Apache Mesos with automatic failover.</li><li>Demonstrated the scheduler running on a Mesos cluster of 150 nodes.</li></ul>
	<b>LLVM Back-end Porting for C*Core Architecture, HEU</b> Sep 2011-Jul 2012 <ul style="list-style-type: none"><li>Devised DAG lowering operations and transformations from LLVM IR.</li><li>Designed selection patterns for 70 insns (totally 100) and optimization passes.</li></ul>
	<b>Research Internship, INRIA-Tsinghua, Beijing</b> Nov 2010-May 2011 <ul style="list-style-type: none"><li>Proposed a compiler-assisted approach to speedup the <b>SimSoC</b> simulator using LLVM Just-In-Time (JIT) engine.</li><li>Exploited a <b>macro-block</b>-based Dynamic Binary Translation (DBT) technique.</li><li>Accelerated 35% in average, and achieved 95 MIPS with peaks at 125 MIPS.</li></ul>
EXTRA-CURRICULARS	<b>President, ACM Student Chapter, UW-Madison</b> 2013-2015 <b>Active Member, Hooper Sailing Club, UW-Madison</b> Aug 2013-present
INTERESTS	Sailing, clarinet, and travel (6 countries).