

# Zuyu (Anthony) Zhang

## Resume

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|-------------------|---|-------------------|
| EDUCATION         | <b>Ph.D. Student, Database Systems</b>  | 2012-present      |
|                   | <b>M.S., Computer Sciences</b>  | 2012-2013         |
|                   | University of Wisconsin-Madison, Madison, WI, USA   |                   |
|                   | <b>M.Eng., Computer Systems Organization</b>  | 2010-2012         |
|                   | Harbin Engineering University (HEU), Harbin, China  |                   |
|                   | <b>B.E., Computer Science and Technology</b>  | 2006-2010         |
|                   | Harbin Institute of Technology (HIT), Harbin, China   |                   |
| TECHNICAL SKILLS  | Prog. Lang.: C/C++, BASH scripts, and X86 AT&T Assembly.<br>Tools: LLVM, SimSoC, DynInst, L <sup>A</sup> T <sub>E</sub> X, GIT, and SVN.  |                   |
| EXPERIENCE        | <b>Teaching Assistant for Computer Network</b> , UW-Madison   | Jan 2014-present  |
|                   | • Grading projects using Mininet, an emulator for Software-Defined Networks.  |                   |
|                   | <b>Selected Course Projects</b> , UW-Madison  | Sep 2012-Dec 2013 |
|                   | • <b>Advanced Operating Systems</b> : Measured performance of Linux virtual memory system, and benchmarked a user-level direct access filesystem for simulated Storage-Class Memory (SCM) using PostMark mail-server workloads. |                   |
|                   | • <b>Distributed Systems</b> : Implemented client and server prototypes for a distributed replicated filesystem using Two-Phase Commit protocol (2PC).  |                   |
|                   | • <b>Principles of Programming Languages</b> : Applied beta reduction in the De Bruijn notation, implemented Algorithm W for type inference, and performed binding-time and function annotation analyses in OCaml.              |                   |
|                   | <b>LLVM Back-end Porting for C*Core Architecture</b> , HEU  | Sep 2011-Jul 2012 |
|                   | • Devised DAG lowering operations and transformations from LLVM IR.   |                   |
|                   | • Designed instruction selection patterns for 70 instructions and optimization passes.  |                   |
|                   | <b>Research Internship</b> , INRIA-Tsinghua, Beijing  | Nov 2010-May 2011 |
|                   | • Proposed a compiler-assisted approach to speedup the <b>SimSoC</b> simulator using LLVM Just-In-Time (JIT) engine.  |                   |
|                   | • Exploited a <b>macro-block</b> -based Dynamic Binary Translation (DBT) technique.   |                   |
|                   | • Accelerated 35% in average, and achieved 95 MIPS with peaks at 125 MIPS.  |                   |
| SCHOLARSHIPS      | <b>1<sup>st</sup> Class Graduate Scholarship</b> , HEU, <b>twice</b>  | 2010-2012         |
|                   | <b>3<sup>rd</sup> Class Scholarship</b> , HIT, <b>twice</b>   | 2007-2009         |
| EXTRA-CURRICULARS | <b>President</b> , ACM Student Chapter, UW-Madison  | 2013-present      |
|                   | <b>President</b> , IBM Technology Club, HIT   | 2009-2010         |
| INTERESTS         | Sailing, skiing, and clarinet.  |                   |