

Zuyu (Anthony) Zhang

Resume

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|-------------------|---|--------------------------|--|
| OBJECTIVE | Seeking for summer internship position on System-related Data Management . | | |
| EDUCATION | Ph.D. student, Computer Sciences | 2012-present | |
| | M.S., Computer Sciences | 2012-Dec 2013 (Expected) | |
| | University of Wisconsin-Madison, Madison, WI, USA | | |
| | M.Eng., Computer Systems Organization | 2010-2012 | |
| | Harbin Engineering University (HEU), Harbin, China | | |
| | Thesis: LLVM based Back-end Porting for C*Core | | |
| | B.Eng., Computer Science and Technology | 2006-2010 | |
| | Harbin Institute of Technology (HIT), Harbin, China | | |
| TECHNICAL SKILLS | Prog. Lang.: C/C++, BASH scripting, X86 AT&T Assembly, and VHDL. Tools: LLVM, SimSoC, DynInst, GIT, SVN, L ^A T _E X, and TiKZ. | | |
| EXPERIENCE | Project Assistant , UW-Madison | Jul 2013-Present | |
| | <ul style="list-style-type: none">• Extracted landscape information from satellite imagery.• Filtered the extracted data set using four machine learning algorithms: Support Vector Machine, k-Nearest Neighbors, Neural Network, and Decision Tree. | | |
| | Research Assistant , UW-Madison | Aug 2012-May 2013 | |
| | <ul style="list-style-type: none">• Performed static analysis and dynamic instrumentation for packed binaries. | | |
| | LLVM Back-end Porting for C*Core Architecture , HEU | Sep 2011-Jul 2012 | |
| | <ul style="list-style-type: none">• Devised DAG lowering operations and transformations from LLVM IR.• Designed selection patterns for 70 instructions and back-end optimization passes.• Produced function prologue/epilogue. | | |
| | Internship , INRIA-Tsinghua, Beijing | Nov 2010-May 2011 | |
| | <ul style="list-style-type: none">• Proposed a macro-block based approach to speedup the SimSoC simulator using LLVM Just-In-Time (JIT) engine.• Accelerated 35% on average and up to 60%. | | |
| PUBLICATIONS | Zuyu Zhang , Vania Joloboff, Xinlei Zhou, Claude Helmstetter, and Guoyin Zhang, “Fast Dynamic Translation Using LLVM On Multi-Core Hosts”, The Fifth Workshop on <i>Architectural and Microarchitectural Support for Binary Translation (AMAS-BT)</i> , in conjunction with ISCA, 2012 | | |
| SCHOLARSHIPS | 1st Class Graduate Scholarship , top 15%, twice, HEU | 2010-2012 | |
| | 3rd Class Scholarship , top 20%, twice, HIT | 2007-2009 | |
| EXTRA-CURRICULARS | Vice President , ACM Student Chapter, UW-Madison | Apr 2013-present | |
| | President , IBM Technology Club, HIT | 2009-2010 | |